NON-VOLATILE RAM PRODUCTS

DATABOOK

1st EDITION

OCTOBER 1995

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

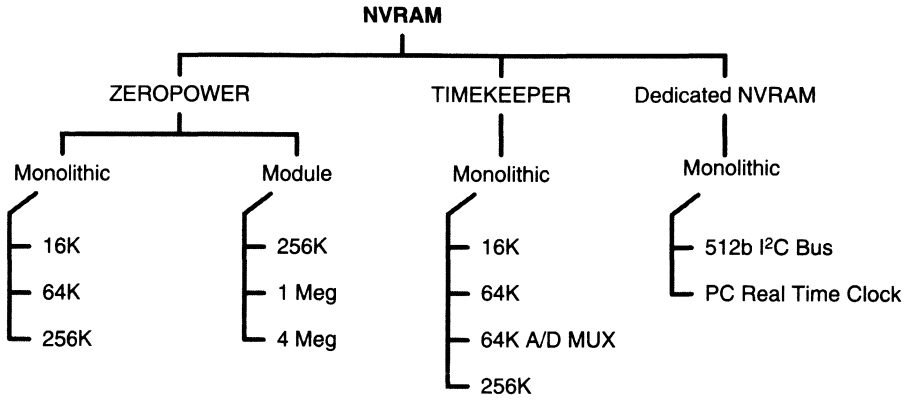
TABLE OF CONTENTS

INTRODUCTION

SGS-THOMSON Microelectronics is a broad range semiconductor company. The product range includes memory products which satisfy the needs of a wide range of applications. They include:

- Non-Volatile Memories: OTP Memories, UV EPROMs, FLASH Memories, Serial and Parallel EEPROMs, and NVRAMs (battery backed SRAMs)
- Synchronous and Asynchronous Fast SRAMs

This databook provides comprehensive technical information on the ZEROPOWER, TIMEKEEPER, and DEDICATED NVRAM Products.



NON-VOLATILE RAM (Battery backed RAM)

NVRAMs satisfy a very important sector of the non-volatile memory market: they provide fast read/write cycles with non-volatile memory for use as data backup. An example of this could be data storage at power failure. The basic ZEROPOWER product consists of an ultra low power SRAM, an integrated supply voltage detect and switchover circuit, and a battery which sustains memory content at power down. The lithium battery has the capacity to maintain the memory contents for up to 10 years in the absence of an external supply. TIMEKEEPER products are similar, but also provide a quartz controlled clock/calendar, which is maintained by the backup battery.

The revolutionary SNAPHAT package provides a surface mount solution for both ZEROPOWER and TIMEKEEPER products. The SNAPHAT consists of two parts, an SO (Small Outline) package which can be mounted by normal surface mounting techniques, and a snap-on battery which can be attached after soldering and washing. This combination allows the lithium battery to be removed for replacement and/or correct environmental disposal.

SGS-THOMSON support an extensive program of both process R & D and product design which generates many new introductions and product updates each year. Please contact your nearest Sales Office to learn about new products that have been introduced since this databook was published.

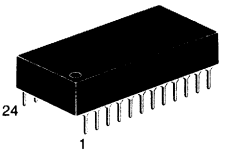
GENERAL INDEX

Note: For Package Drawings refer to individual Data Sheet.

ZEROPOWER RAM

CMOS 2K x 8 ZEROPOWER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- UNLIMITED WRITE CYCLES
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z02: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z12: 4.2V ≤ V_{PFD} ≤ 4.5V
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 2K x 8 SRAMs



PCDIP24 (PC)
Battery CAPHAT

DESCRIPTION

The M48Z02,12 ZEROPOWER® RAM is a 2K x 8 non-volatile static RAM which is pin and functional compatible with the MK48Z02,12.

A special 24 pin 600mil DIP CAPHAT™ package houses the M48Z02,12 silicon with a long life lithium button cell to form a highly integrated battery backed-up memory solution.

Table 1. Signal Names

A0-A10	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

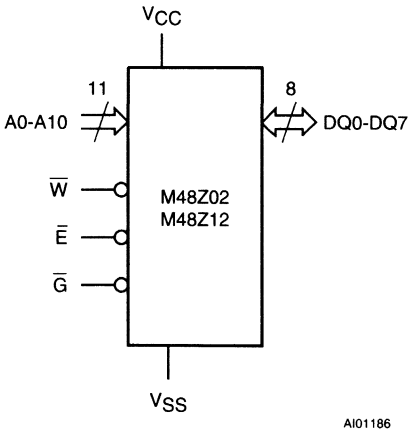


Table 2. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature (V_{CC} Off)		–40 to 85	°C
V_{IO}	Input or Output Voltages		–0.3 to 7	V
V_{CC}	Supply Voltage		–0.3 to 7	V
I_O	Output Current		20	mA
P_D	Power Dissipation		1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

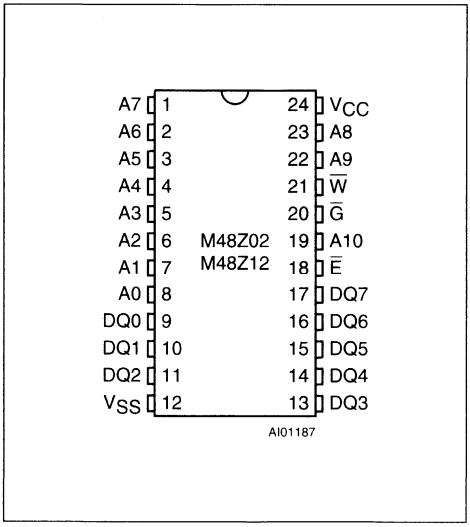
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections



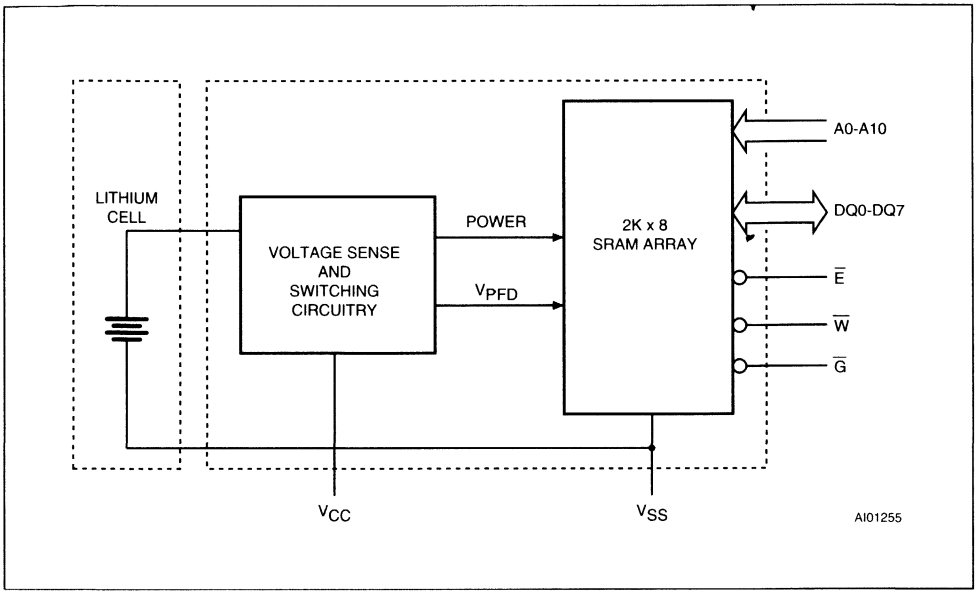
DESCRIPTION (cont'd)

The M48Z02,12 button cell has sufficient capacity and storage life to maintain data and clock functionality for an accumulated time period of at least 10 years in the absence of power over the operating temperature range.

The M48Z02,12 is a non-volatile pin and function equivalent to any JEDEC standard 2K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z02,12 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

Figure 3. Block Diagram



READ MODE

The M48Z02,12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs defines which one of the 2,048 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0.6V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

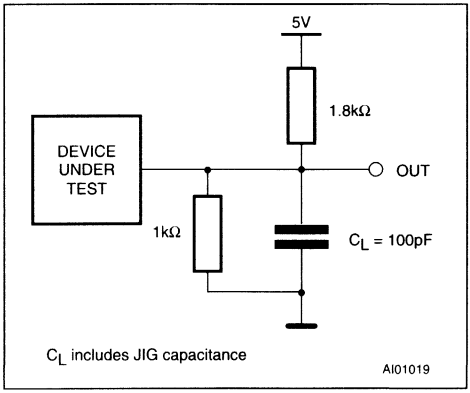


Table 4. Capacitance [1] (T_A = 25 °C)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [2]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with ΔV = 3V and power supply at 5V.
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO} [1]	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±5	µA
I_{CC}	Supply Current	Outputs open		80	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} - 0.2V$		3	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs Deselected.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C or –40 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z02)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z12)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR}	Expected Data Retention Time	10			YEARS

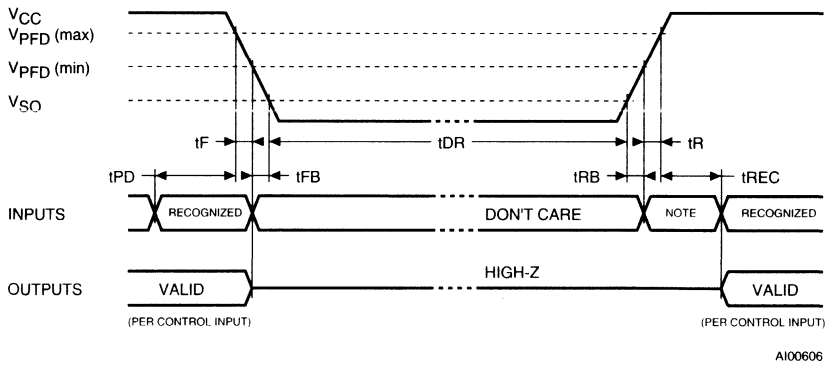
Note: 1. All voltages referenced to V_{SS}.

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C or –40 to 85°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 50 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PFD}(min). Some systems may performs inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

Table 8. Read Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z02 / 12						Unit
		-120		-150		-200		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	120		150		200		ns
t_{AVQV}	Address Valid to Output Valid		120		150		200	ns
t_{ELQV}	Chip Enable Low to Output Valid		120		150		200	ns
t_{GLQV}	Output Enable Low to Output Valid		75		75		80	ns
t_{ELQX}	Chip Enable Low to Output Transition	10		10		10		ns
t_{GLQX}	Output Enable Low to Output Transition	5		5		5		ns
t_{EHQZ}	Chip Enable High to Output Hi-Z		30		35		40	ns
t_{GHQZ}	Output Enable High to Output Hi-Z		30		35		40	ns
t_{AXQX}	Address Transition to Output Transition	5		5		5		ns

Figure 6. Read Mode AC Waveforms

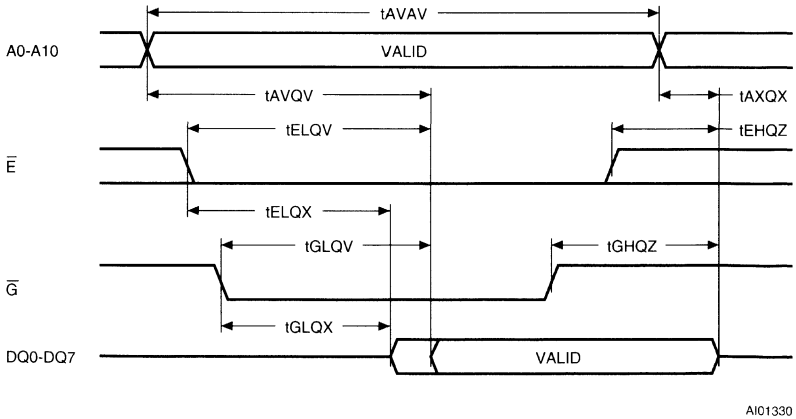


Table 9. Write Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z02 / 12						Unit
		-120		-150		-200		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	120		150		200		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{WLWH}	Write Enable Pulse Width	75		90		120		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	75		90		120		ns
t_{WHAX}	Write Enable High to Address Transition	10		10		10		ns
t_{EHAX}	Chip Enable High to Address Transition	10		10		10		ns
t_{DVWH}	Input Valid to Write Enable High	35		40		60		ns
t_{DVEH}	Input Valid to Chip Enable High	35		40		60		ns
t_{WHDX}	Write Enable High to Input Transition	5		5		5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		5		5		ns
t_{WLQZ}	Write Enable Low to Output Hi-Z		40		50		60	ns
t_{AVWH}	Address Valid to Write Enable High	90		120		140		ns
t_{AVEH}	Address Valid to Chip Enable High	90		120		140		ns
t_{WHQX}	Write Enable High to Output Transition	10		10		10		ns

WRITE MODE

The M48Z02,12 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 7. Write Enable Controlled, Write AC Waveforms

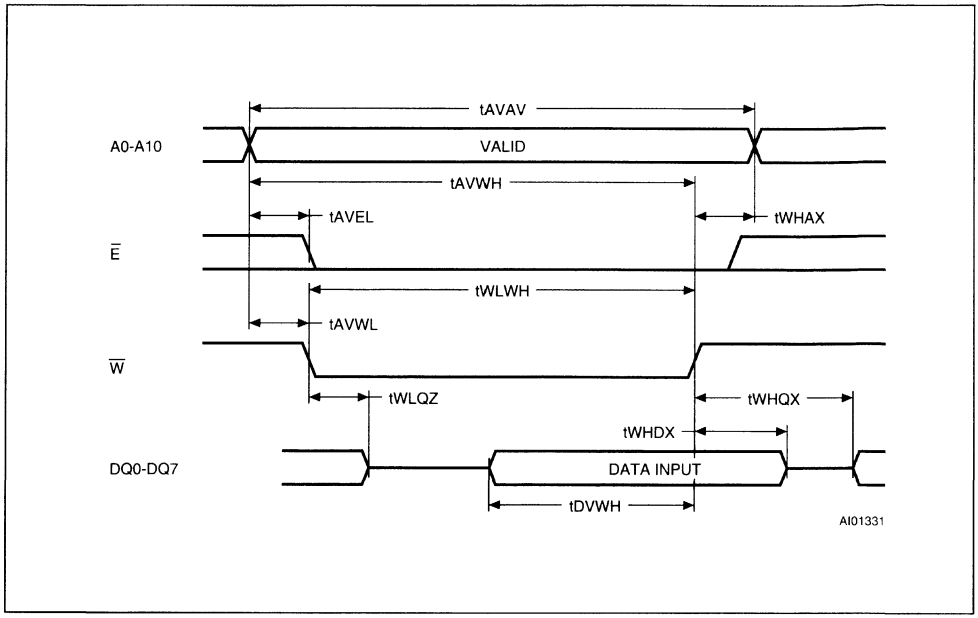
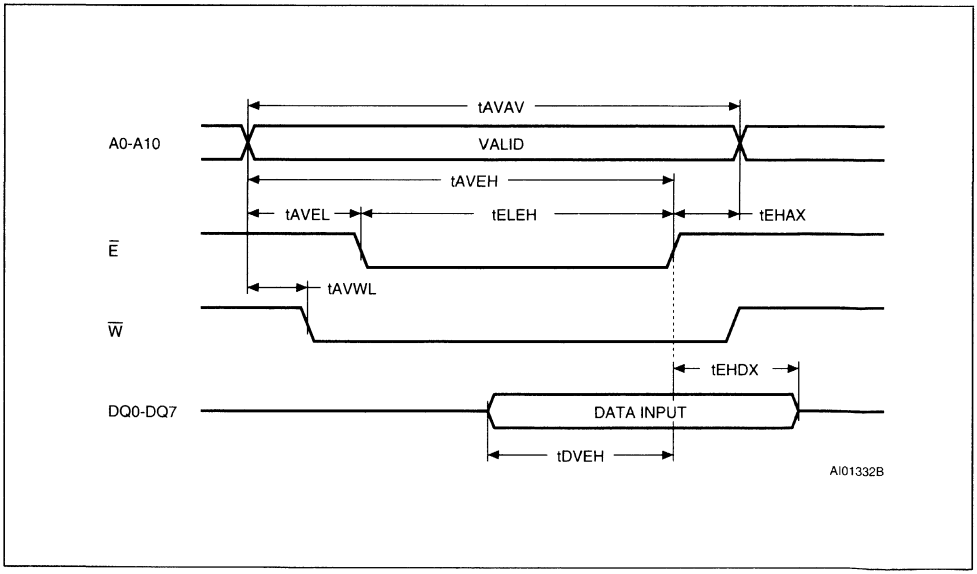


Figure 8. Chip Enable Controlled, Write AC Waveforms



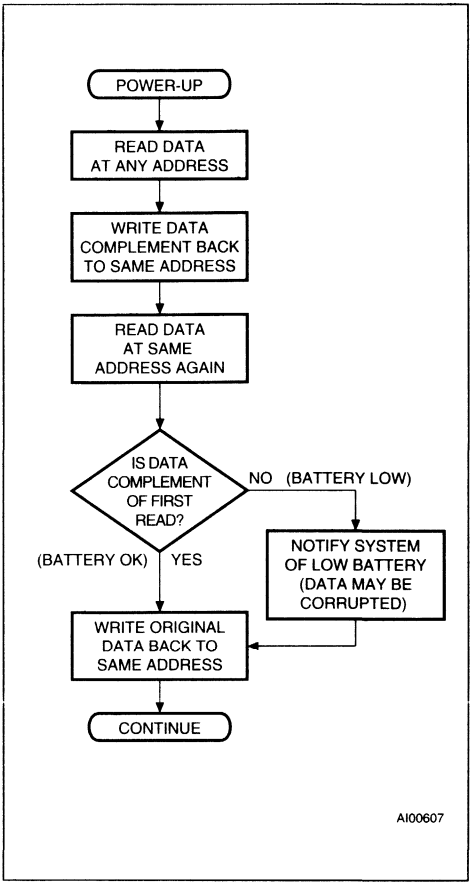
DATA RETENTION MODE

With valid V_{CC} applied, the M48Z02,12 operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

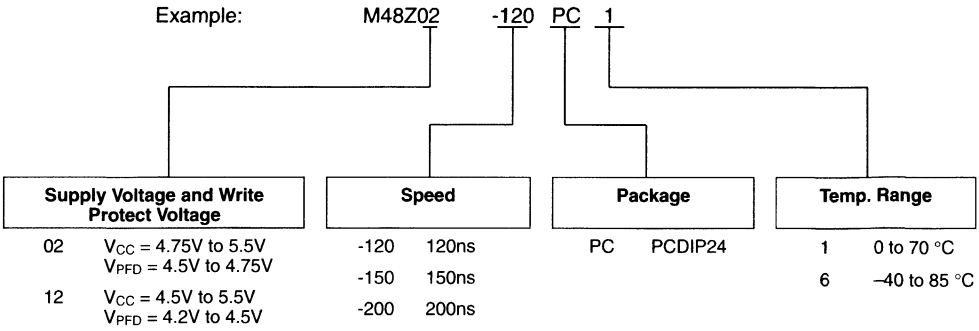
Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z02,12 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises, the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 9 illustrates how a $\overline{BOK}$ check routine could be structured.

Figure 9. Checking the $\overline{BOK}$ Flag Status



ORDERING INFORMATION SCHEME



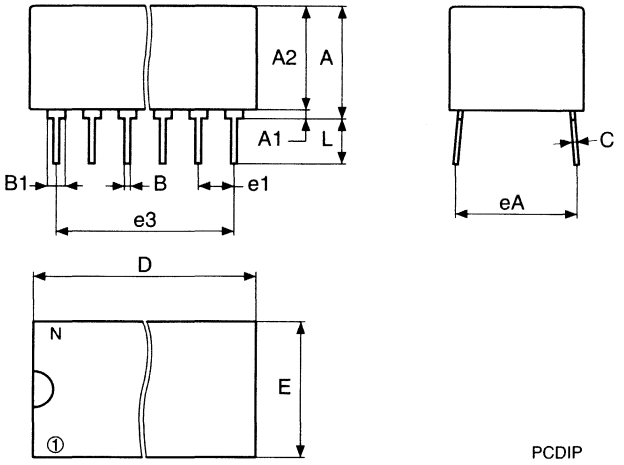
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP24 - 24 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.36	8.89		0.329	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		34.29	34.80		1.350	1.370
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		25.15	30.73		0.990	1.210
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	24			24		

PCDIP24

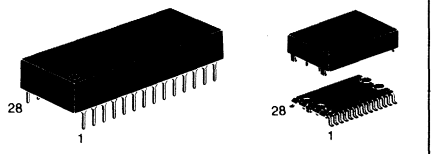


PCDIP

Drawing is not to scale

CMOS 8K x 8 ZEROPOWER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- UNLIMITED WRITE CYCLES
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z08: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z18: 4.2V ≤ V_{PFD} ≤ 4.5V
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY
- SNAPHAT HOUSING (BATTERY) REPLACEABLE
- 11 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with the MK48Z08, 18 and JEDEC STANDARD 8K x 8 SRAMs



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

DESCRIPTION

The M48Z08,18 ZEOPOWER® RAM is an 8K x 8 non-volatile static RAM which is pin and functional compatible with the MK48Z08,18. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory solution.

Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

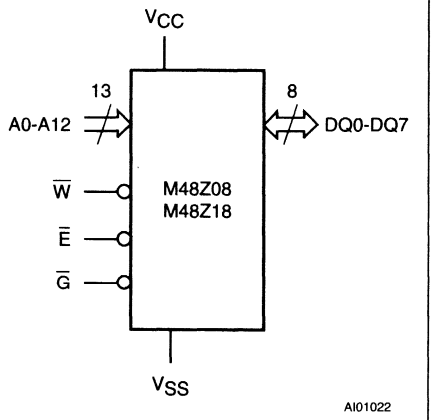
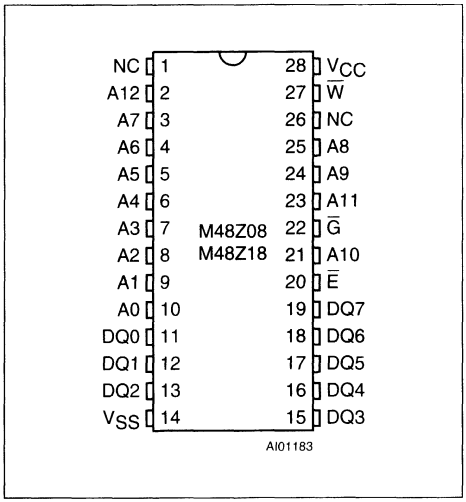
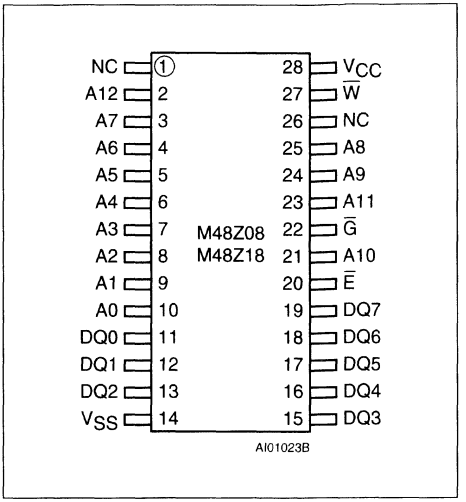


Figure 2A. DIP Pin Connections



Warning: NC = No Connection

Figure 2B. SO Pin Connections



Warning: NC = No Connection

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

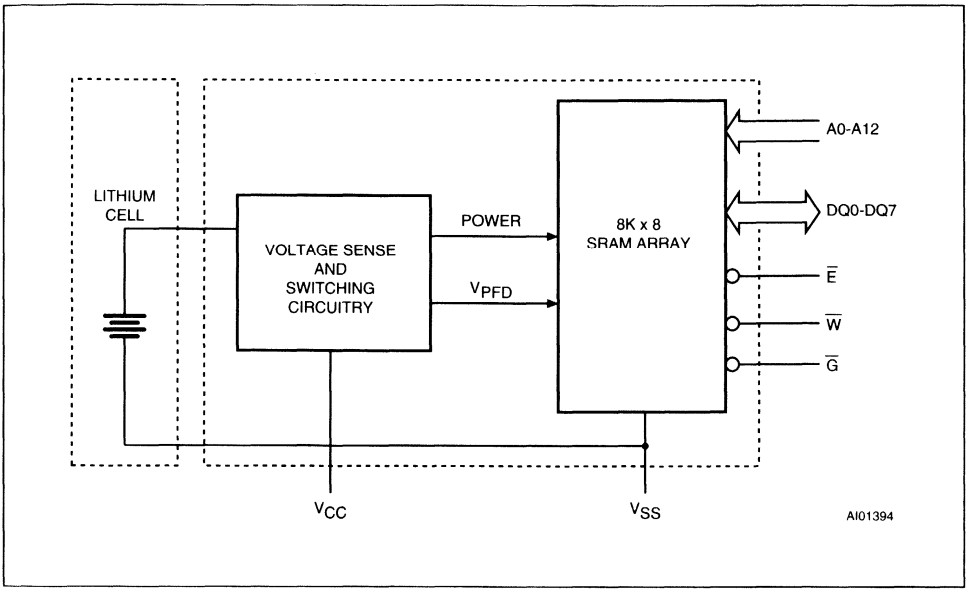
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 3. Block Diagram



DESCRIPTION (cont'd)

The M48Z08,18 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 28 pin 600mil DIP CAPHAT™ houses the M48Z08,18 silicon with a long life lithium button cell in a single package.

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

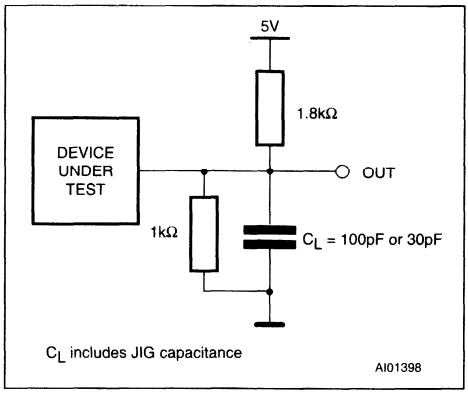


Table 4. Capacitance [1] (T_A = 25 °C)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [2]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance calculated from the equation C = IΔt/ΔV with ΔV = 3V and power supply at 5V.
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		80	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ = V_{CC} – 0.2V		3	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z08)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z18)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR}	Expected Data Retention Time	11			YEARS

Note: 1. All voltages referenced to V_{SS}.

DESCRIPTION (cont'd)

For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4Z28-BR00SH1".

The M48Z08,18 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition.

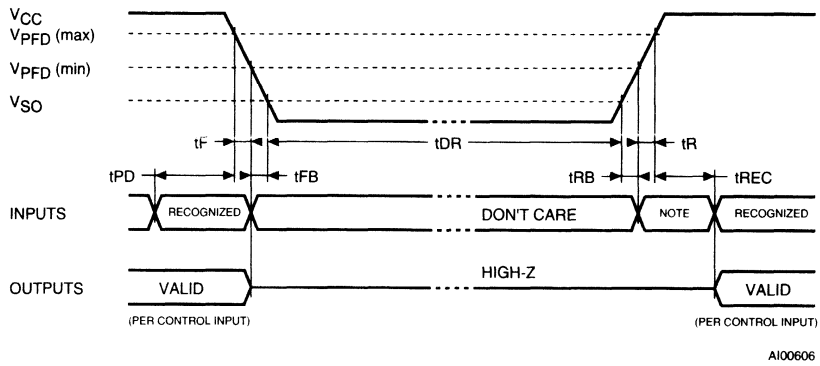
When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data until valid power returns.

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	1		ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PFD}(min). Some systems may performs inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z08 / 18 -100		Unit
		Min	Max	
t_{AVAV}	Read Cycle Time	100		ns
t_{AVQV} (1)	Address Valid to Output Valid		100	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		100	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		50	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	10		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		50	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		40	ns
t_{AXQX} (1)	Address Transition to Output Transition	5		ns

Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 30pF (see Figure 4).

Figure 6. Read Mode AC Waveforms

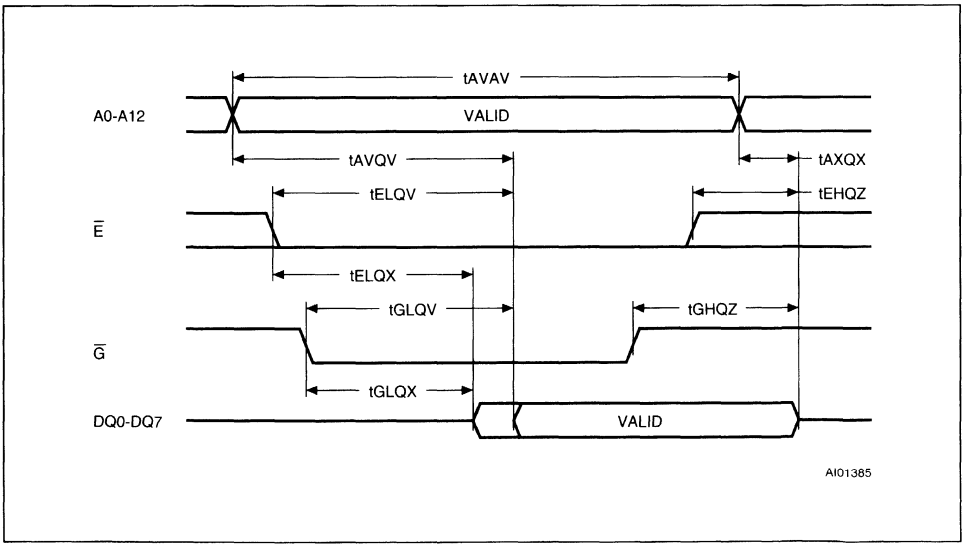


Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z08 / 18 -100		Unit
		Min	Max	
t_{AVAV}	Write Cycle Time	100		ns
t_{AVWL}	Address Valid to Write Enable Low	0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		ns
t_{WLWH}	Write Enable Pulse Width	80		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	80		ns
t_{WHAX}	Write Enable High to Address Transition	10		ns
t_{EHAX}	Chip Enable High to Address Transition	10		ns
t_{DVWH}	Input Valid to Write Enable High	50		ns
t_{DVEH}	Input Valid to Chip Enable High	30		ns
t_{WHDX}	Write Enable High to Input Transition	5		ns
t_{E1HDX}	Chip Enable High to Input Transition	5		ns
t_{WLQZ} (1, 2)	Write Enable Low to Output Hi-Z		50	ns
t_{AVWH}	Address Valid to Write Enable High	80		ns
t_{AVEH}	Address Valid to Chip Enable High	80		ns
t_{WHQX} (1, 2)	Write Enable High to Output Transition	10		ns

Notes: 1. C_L= 30pF (see Figure 4).
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

READ MODE

The M48Z08,18 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple- through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48Z08,18 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$.

A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 7. Write Enable Controlled, Write AC Waveforms

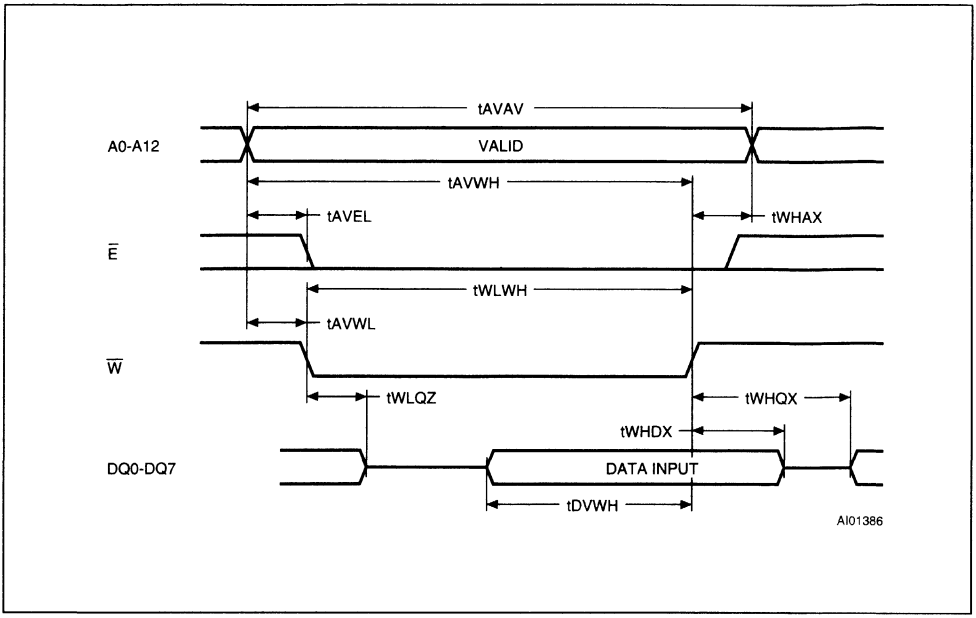
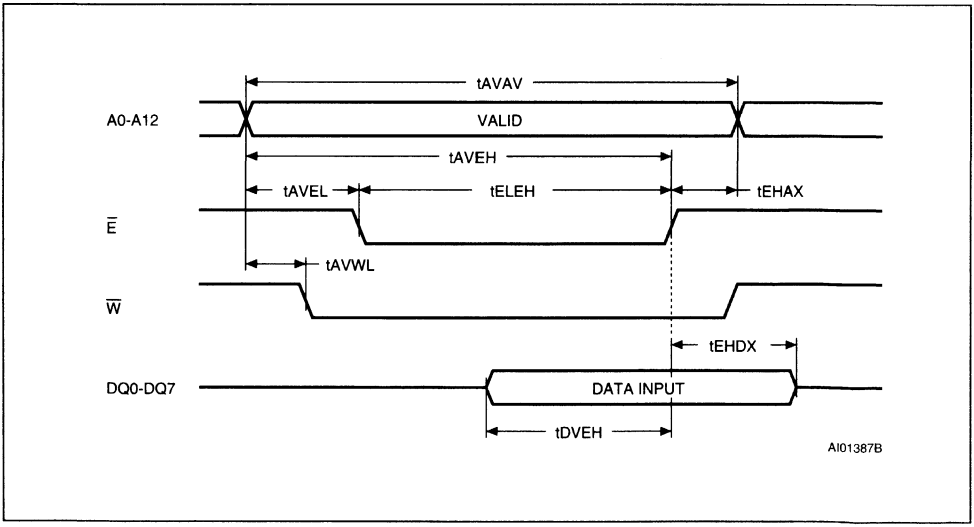


Figure 8. Chip Enable Controlled, Write AC Waveforms



DATA RETENTION MODE

With valid V_{CC} applied, the M48Z08,18 operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

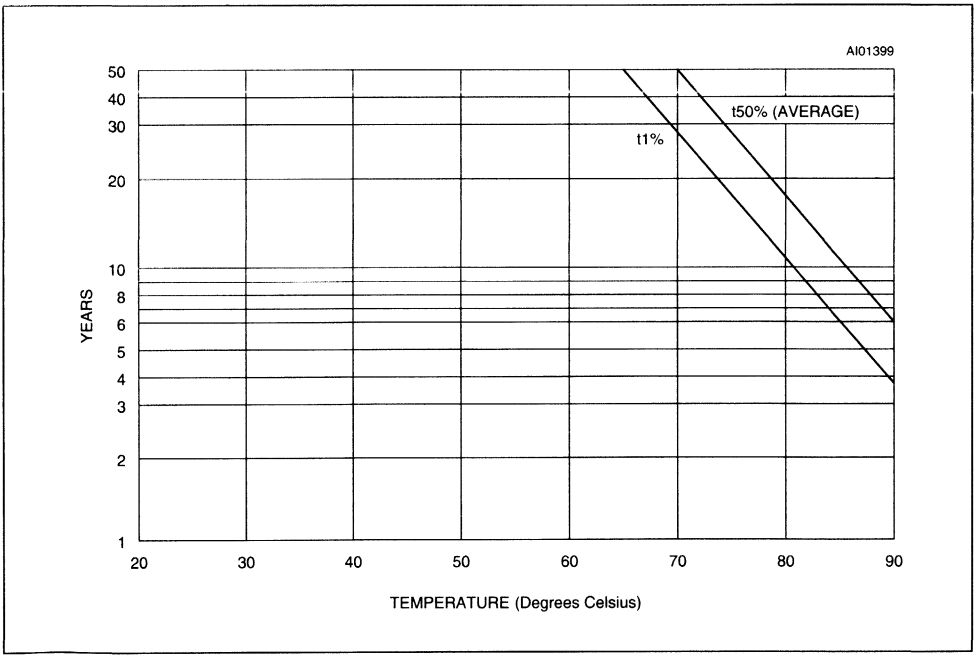
Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z08,18 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48Z08,18 for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD}(min). $\overline{E}$ should be kept high as V_{CC} rises past V_{PFD}(min) to prevent inadvertent write cycles prior to processor stabilization. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max).

SYSTEM BATTERY LIFE

The useful life of the battery in the M48Z08,18 is expected to ultimately come to an end for one of two reasons: either because it has been discharged while providing current to the RAM in the battery back-up mode, or because the effects of aging render the cell useless before it can actually be completely discharged. The two effects are virtually unrelated allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms. The earlier occurring failure mechanism defines the battery system life of the M48Z08,18.

Figure 9. Predicted Battery Storage Life versus Temperature



Cell Storage Life

Storage life is primarily a function of temperature. Figure 9 illustrates the approximate storage life of the M48Z08,18 battery over temperature. The results in Figure 9 are derived from temperature accelerated life test studies performed at SGS-THOMSON. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4V closed circuit voltage across a 250 kΩ load resistor. The two lines, $t_{1\%}$ and $t_{50\%}$, represent different failure rate distributions for the cell's storage life. At 70°C, for example, the $t_{1\%}$ line indicates that an M48Z08,18 has a 1% chance of having a battery failure 28 years into its life while the $t_{50\%}$ shows the part has a 50% chance of failure at the 50 year mark. The $t_{1\%}$ line represents the practical onset of wear out and can be considered the worst case Storage Life for the cell. The $t_{50\%}$ can be considered the normal or average life.

Calculating Storage Life

The following formula can be used to predict storage life:

$$\frac{1}{\{[(TA1/TT)/SL1]+[(TA2/TT)/SL2]+...+[(TAN/TT)/SLN]\}}$$

where,

- TA1, TA2, TAN = time at ambient temperature 1, 2, etc.
- TT = total time = TA1+TA2+...+TAN
- SL1, SL2, SLN = storage life at temperature 1, 2, etc.

For example an M48Z08,18 is exposed to temperatures of 55°C or less for 8322 hrs/yr, and temperatures greater than 60°C but less than 70°C for the remaining 438 hrs/yr. Reading predicted $t_{1\%}$ values from Figure 9,

- SL1 ≅ 200 yrs, SL2 = 28 yrs
- TT = 8760 hrs/yr
- TA1 = 8322 hrs/yr, TA2 = 438 hrs/yr

Predicted storage life ≥

$$\frac{1}{\{[(8322/8760)/200]+[(431/8760)/28]\}}$$

or 154 years.

As can been seen from these calculations and the results, the expected lifetime of the M48Z08, 18 should exced most system requirements.

Estimated System Life

Since either storage life or capacity consumption can end the battery's life, the system life is marked by which ever occurs first.

Reference for System Life

Each M48Z08,18 is marked with a nine digit manufacturing date code in the form of H99XXYYZZ. For example, H995B9431 is:

H = fabricated in Carrollton, TX

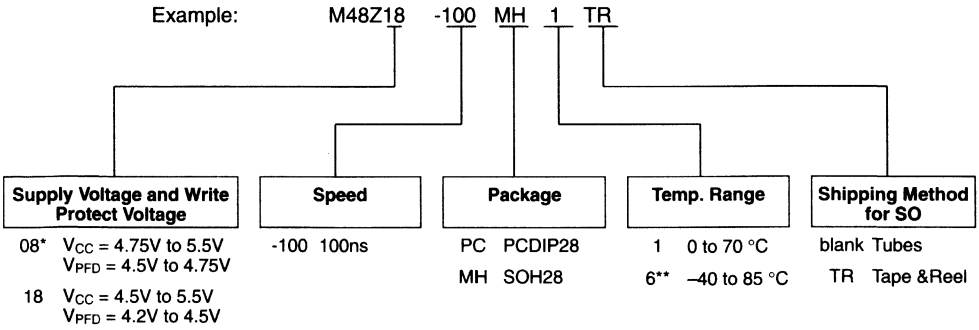
9 = assembled in Muar, Malaysia,

9 = tested in Muar, Malaysia,

5B = lot designator,

9431 = assembled in the year 1994, work week 31.

ORDERING INFORMATION SCHEME



Notes: 08* CAPHAT package only.
6** Temperature range available for M48Z18 product only.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the M48T18 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4Z28-BR00SH1".

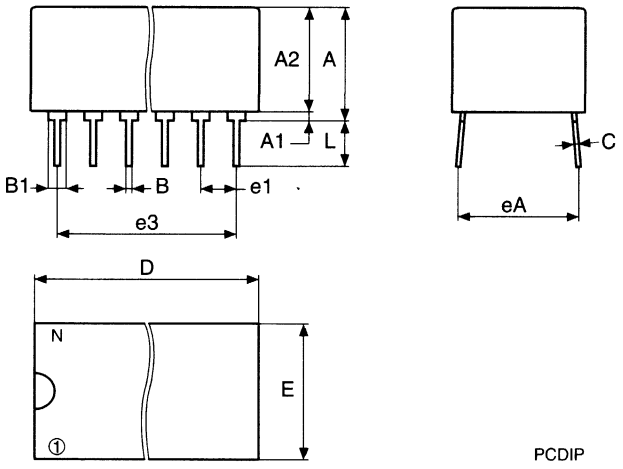
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP28 - 28 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

PCDIP28



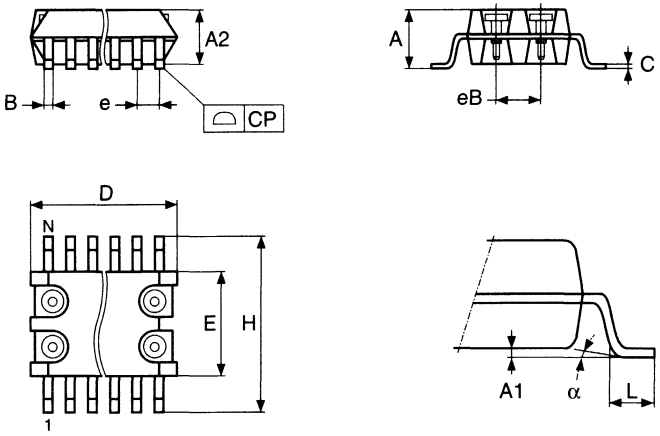
PCDIP

Drawing is not to scale

SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N		28			28	
CP			0.10			0.004

SOH28



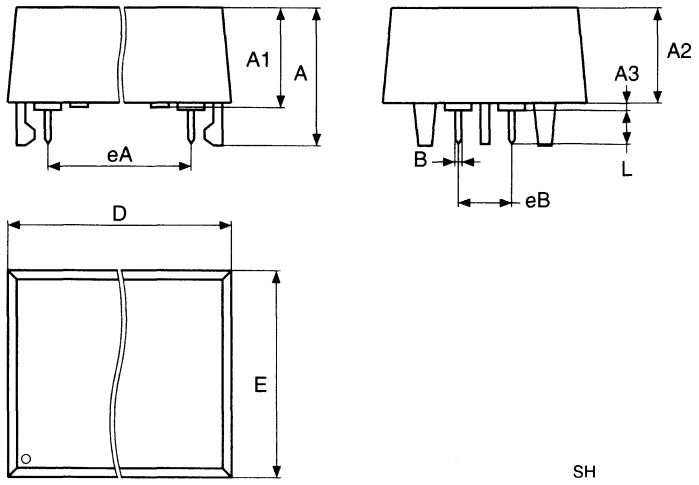
SOH

Drawing not to scale

SH28 - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

SH28



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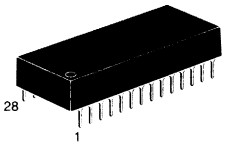
CMOS 8K x 8 ZEROPOWER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- UNLIMITED WRITE CYCLES
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- POWER-FAIL INTERRUPT
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z09: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z19: 4.2V ≤ V_{PFD} ≤ 4.5V
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- 11 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with the MK48Z09, 19 and JEDEC STANDARD 8K x 8 SRAMs



PCDIP28 (PC)
Battery CAPHAT

DESCRIPTION

The M48Z09,19 ZEROPOWER® RAM is an 8K x 8 non-volatile static RAM which is pin and function compatible with the MK48Z09,19.

A special 28 pin 600mil DIP CAPHAT™ package houses the M48Z09,19 silicon with a long life lithium button cell to form a highly integrated battery backed-up memory solution.

Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{INT}$	Power Fail Interrupt
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

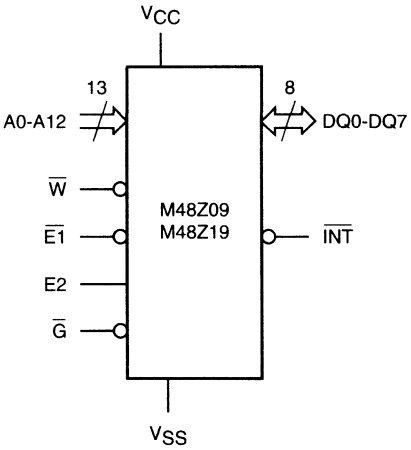


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

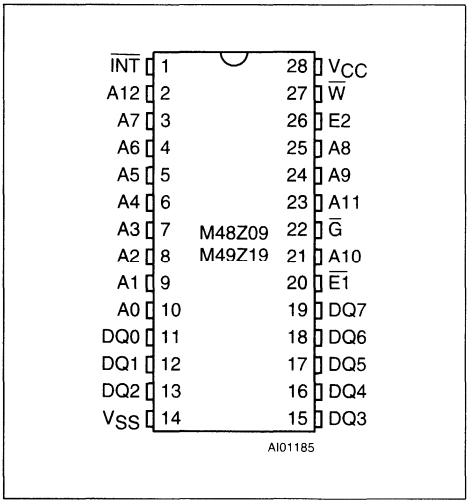
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	X	High Z	Standby
Deselect		X	V_{IL}	X	X	High Z	Standby
Write		V_{IL}	V_{IH}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2A. DIP Pin Connections



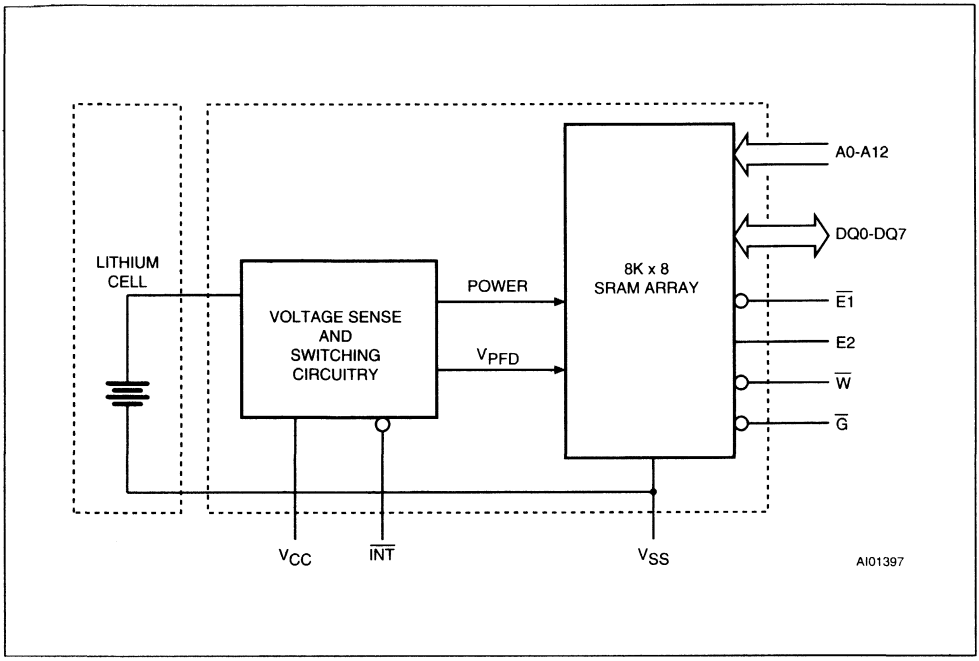
DESCRIPTION (cont'd)

The M48Z09,19 button cell has sufficient capacity and storage life to maintain data for an accumulated time period of at least 11 years in the absence of power over the operating temperature range.

The M48Z09,19 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z09,19 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

Figure 3. Block Diagram



READ MODE

The M48Z09,19 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E1}$ (Chip Enable 1) is low, and E2 (Chip Enable 2) is high. The device architecture allows ripple- through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E1}$, E2, and $\overline{G}$ access times are also satisfied. If the $\overline{E1}$, E2 and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Times (t_{E1LQV} or t_{E2HQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E1}$, E2 and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E1}$, E2 and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

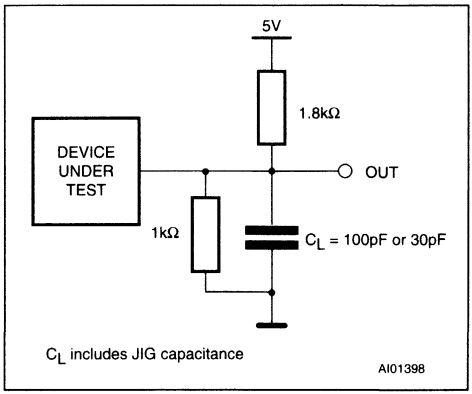


Table 4. Capacitance [1] (T_A = 25 °C)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [2]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with ΔV = 3V and power supply at 5V.
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		80	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E1}$ = V_{IH}, E2 = V_{IL}		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E1}$ = V_{CC} – 0.2V, E2 = V_{SS} + 0.2V		3	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
	Output Low Voltage ($\overline{INT}$) [1]	I_{OL} = 0.5mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. The $\overline{INT}$ pin is Open Drain.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z09)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z19)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR}	Expected Data Retention Time	11			YEARS

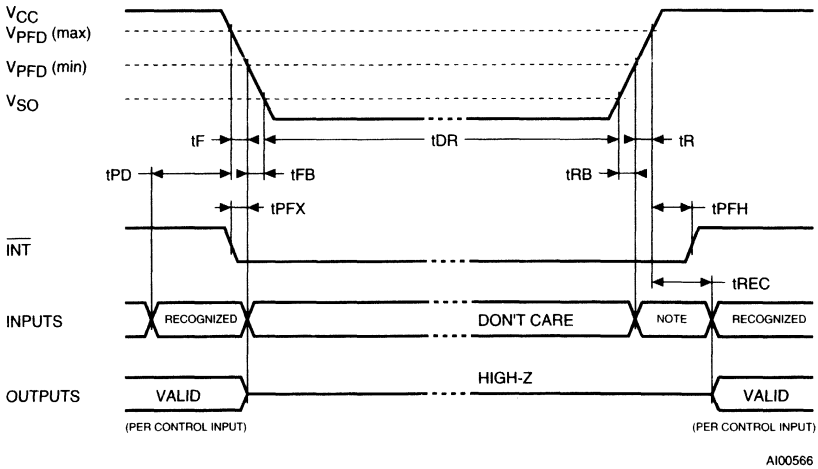
Note: 1. All voltages referenced to V_{SS}.

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E1}$ or $\overline{W}$ at V_{IH} or E2 at V_{IL} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	$\overline{E1}$ or $\overline{W}$ at V_{IH} or E2 at V_{IL} after Power Up	1		ms
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	µs
t_{PFH} (3)	V_{PFD} (max) to $\overline{INT}$ High		120	µs

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.
3. $\overline{INT}$ may go high anytime after V_{CC} exceeds V_{PFD} (min) and is guaranteed to go high t_{PFH} after V_{CC} exceeds V_{PFD} (max).

Figure 5. Power Down/Up Mode AC Waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E1}$ high or E2 low as V_{CC} rises past V_{PFD}(min). Some systems may performs inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z09 / 19 -100		Unit
		Min	Max	
t_{AVAV}	Read Cycle Time	100		ns
t_{AVQV} (1)	Address Valid to Output Valid		100	ns
t_{E1LQV} (1)	Chip Enable 1 Low to Output Valid		100	ns
t_{E2HQV} (1)	Chip Enable 2 High to Output Valid		100	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		50	ns
t_{E1LQX} (2)	Chip Enable 1 Low to Output Transition	10		ns
t_{E2HQX} (2)	Chip Enable 2 High to Output Transition	10		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		ns
t_{E1HQZ} (2)	Chip Enable 1 High to Output Hi-Z		50	ns
t_{E2LQZ} (2)	Chip Enable 2 Low to Output Hi-Z		50	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		40	ns
t_{AXQX} (1)	Address Transition to Output Transition	5		ns

Notes: 1. C_L= 100pF (see Figure 4).
2. C_L= 30pF (see Figure 4)

Figure 6. Read Mode AC Waveforms

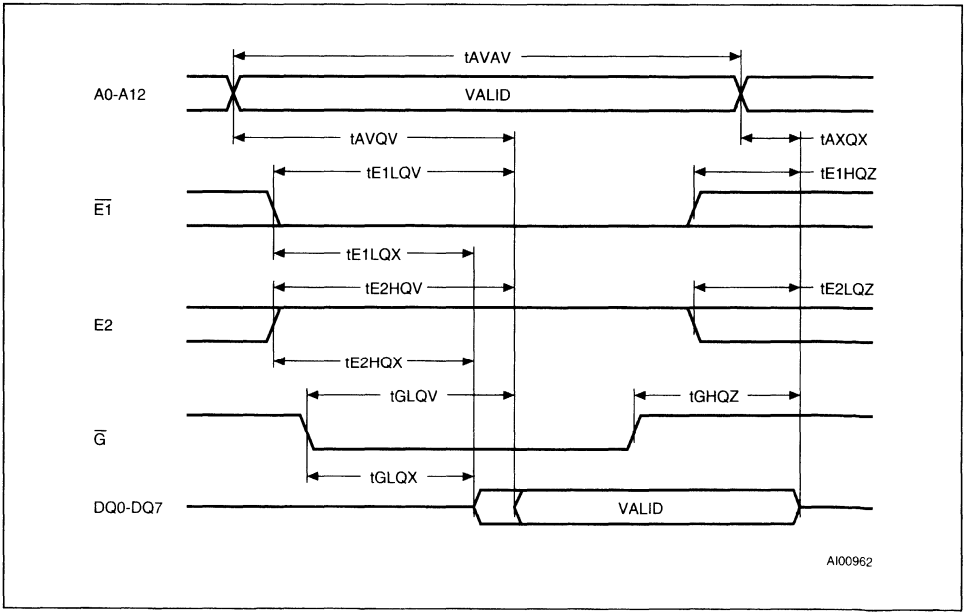


Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z09 / 19		Unit
		-100		
		Min	Max	
t_{AVAV}	Write Cycle Time	100		ns
t_{AVWL}	Address Valid to Write Enable Low	0		ns
t_{AVE1L}	Address Valid to Chip Enable 1 Low	0		ns
t_{AVE2H}	Address Valid to Chip Enable 2 High	0		ns
t_{WLWH}	Write Enable Pulse Width	80		ns
t_{E1LE1H}	Chip Enable 1 Low to Chip Enable 1 High	80		ns
t_{E2HE2L}	Chip Enable 2 High to Chip Enable 2 Low	80		ns
t_{WHAX}	Write Enable High to Address Transition	10		ns
t_{E1HAX}	Chip Enable 1 High to Address Transition	10		ns
t_{E2LAX}	Chip Enable 2 Low to Address Transition	10		ns
t_{DVWH}	Input Valid to Write Enable High	50		ns
t_{DVE1H}	Input Valid to Chip Enable 1 High	50		ns
t_{DVE2L}	Input Valid to Chip Enable 2 Low	50		ns
t_{WHDX}	Write Enable High to Input Transition	5		ns
t_{E1HDX}	Chip Enable 1 High to Input Transition	5		ns
t_{E2LDX}	Chip Enable 2 Low to Input Transition	5		ns
t_{WLQZ} (1, 2)	Write Enable Low to Output Hi-Z		50	ns
t_{AVWH}	Address Valid to Write Enable High	80		ns
t_{AVE1H}	Address Valid to Chip Enable 1 High	80		ns
t_{AVE2L}	Address Valid to Chip Enable 2 Low	80		ns
t_{WHQX} (1, 2)	Write Enable High to Output Transition	10		ns

Notes: 1. C_L= 30pF (see Figure 4).
2. If E1 goes low or E2 high simultaneously with W going low, the outputs remain in the high impedance state.

Figure 7. Write Enable Controlled, Write AC Waveforms

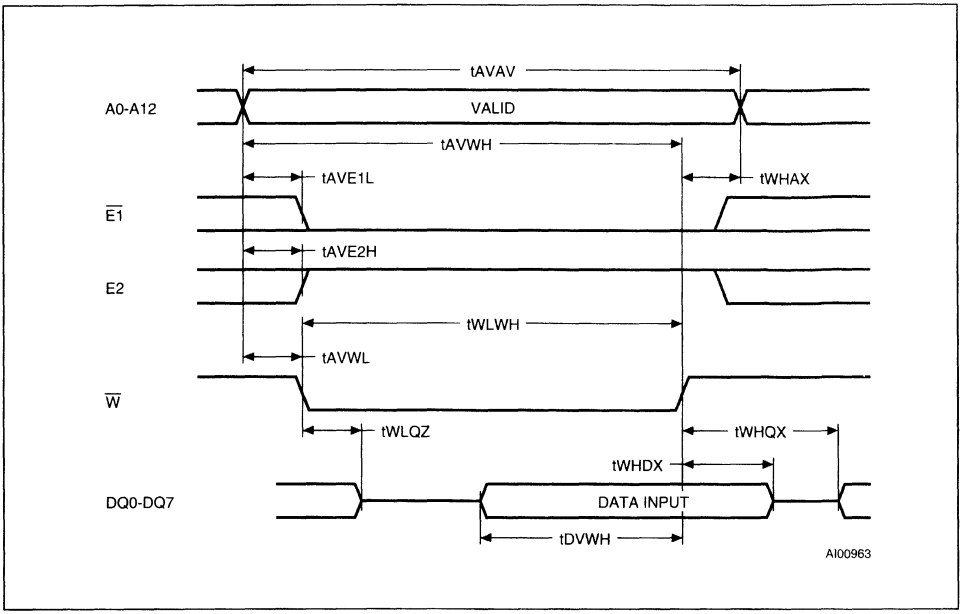
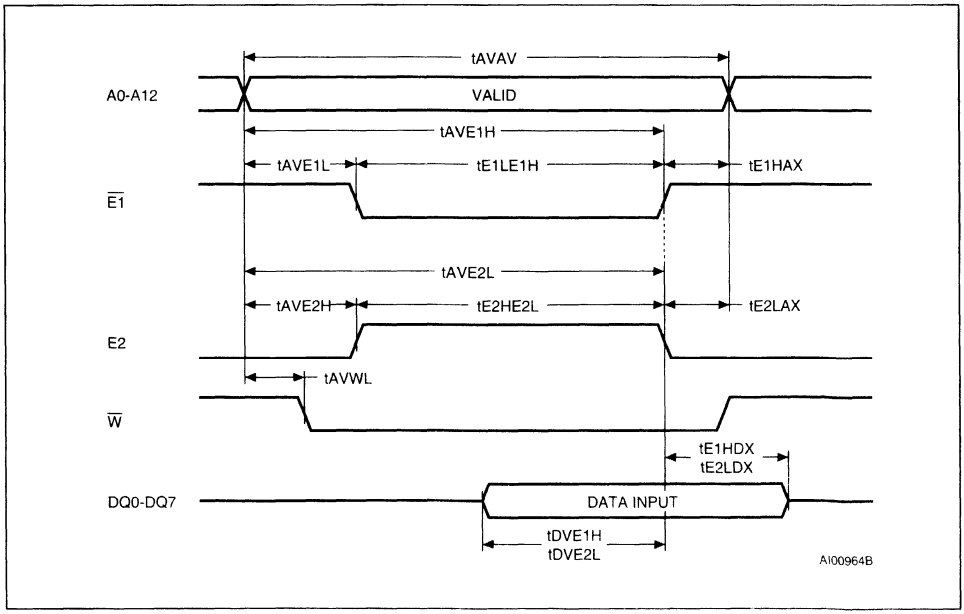


Figure 8. Chip Enable Controlled, Write AC Waveforms



WRITE MODE

The M48Z09,19 is in the Write Mode whenever $\overline{W}$, $\overline{E1}$, and E2 are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E1}$, or the rising edge of E2. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E1}$, or the falling edge of E2. The addresses must be held valid throughout the cycle. $\overline{E1}$ or $\overline{W}$ must return high or E2 low for minimum of t_{E1HAX} or t_{E2LAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E1}$ and $\overline{G}$ and a high on E2, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48Z09,19 operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z09,19 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48Z09,19 for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD}(min). $\overline{E1}$ should be kept high or E2 low as V_{CC} rises past V_{PFD}(min) to prevent inadvertent write cycles prior to processor stabilization. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max).

POWER FAIL INTERRUPT PIN

The M48Z09,19 continuously monitors V_{CC}. When V_{CC} falls to the power-fail detect trip point, an interrupt is immediately generated. An internal clock provides a delay of between 10µs and 40µs before automatically deselecting the M48Z09,19. The $\overline{INT}$ pin is an open drain output and requires an external pull up resistor, even if the interrupt output function is not being used.

SYSTEM BATTERY LIFE

The useful life of the battery in the M48Z09,19 is expected to ultimately come to an end for one of two reasons: either because it has been discharged while providing current to the RAM in the battery back-up mode, or because the effects of aging render the cell useless before it can actually be completely discharged. The two effects are virtually unrelated allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms. The earlier occurring failure mechanism defines the battery system life of the M48Z09,19.

Cell Storage Life

Storage life is primarily a function of temperature. Figure 9 illustrates the approximate storage life of the M48Z09,19 battery over temperature. The results in Figure 9 are derived from temperature accelerated life test studies performed at SGS-THOMSON. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4V closed circuit voltage across a 250 kΩ load resistor. The two lines, $t_{1\%}$ and $t_{50\%}$, represent different failure rate distributions for the cell's storage life. At 70°C, for example, the $t_{1\%}$ line indicates that an M48Z09,19 has a 1% chance of having a battery failure 28 years into its life while the $t_{50\%}$ shows the part has a 50% chance of failure at the 50 year mark. The $t_{1\%}$ line represents the practical onset of wear out and can be considered the worst case Storage Life for the cell. The $t_{50\%}$ can be considered the normal or average life.

Calculating Storage Life

The following formula can be used to predict storage life:

$$\frac{1}{\{[(TA1/TT)/SL1]+[(TA2/TT)/SL2]+...+[(TAN/TT)/SLN]\}}$$

where,

- TA1, TA2, TAN = time at ambient temperature 1, 2, etc.
- TT = total time = TA1+TA2+...+TAN
- SL1, SL2, SLN = storage life at temperature 1, 2, etc.

For example an M48Z09,19 is exposed to temperatures of 55°C or less for 8322 hrs/yr, and temperatures greater than 60°C but less than 70°C for the remaining 438 hrs/yr. Reading predicted $t_{1\%}$ values from Figure 9,

- SL1 ≅ 200 yrs, SL2 = 28 yrs
- TT = 8760 hrs/yr
- TA1 = 8322 hrs/yr, TA2 = 438 hrs/yr

Predicted storage life ≥

$$\frac{1}{\{[(8322/8760)/200]+[(431/8760)/28]\}}$$

or 154 years.

As can be seen from these calculations and the results, the expected life time of the M48Z09, 19 should exceed most system requirements.

Estimated System Life

Since either storage life or capacity consumption can end the battery's life, the system life is marked by which ever occurs first.

Reference for System Life

Each M48Z09,19 is marked with a nine digit manufacturing date code in the form of H99XXYYZZ. For example, H995B9431 is:

H = fabricated in Carrollton, TX

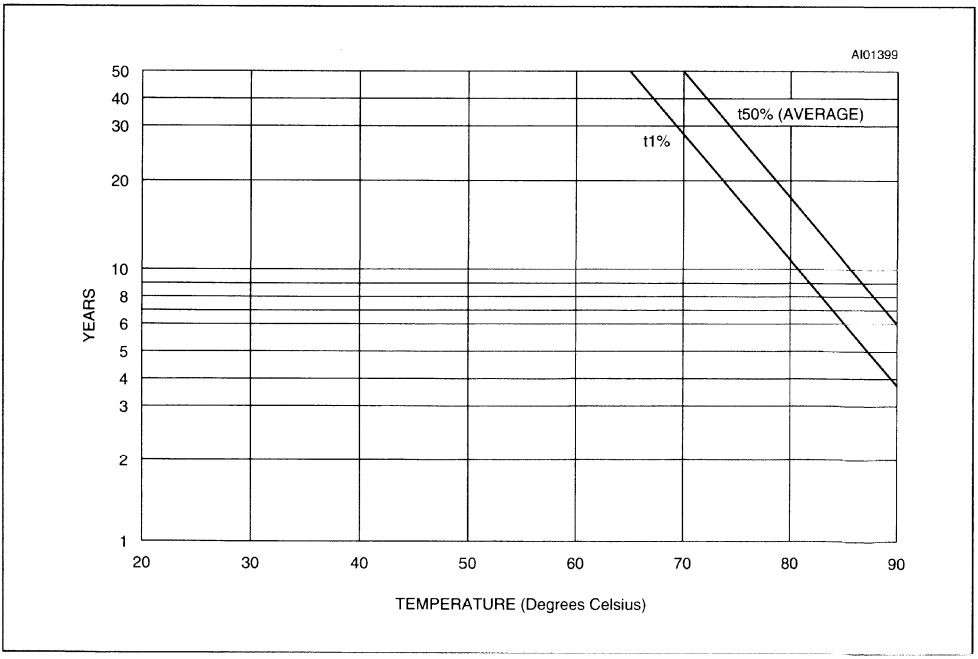
9 = assembled in Muar, Malaysia,

9 = tested in Muar, Malaysia,

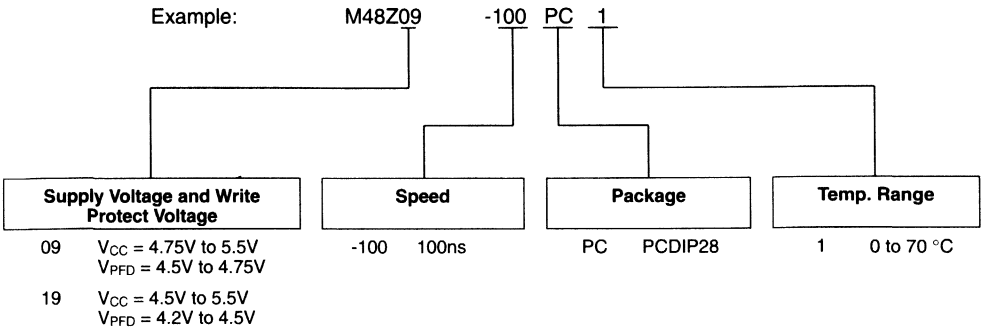
5B = lot designator,

9431 = assembled in the year 1994, work week 31.

Figure 9. Predicted Battery Storage Life versus Temperature



ORDERING INFORMATION SCHEME



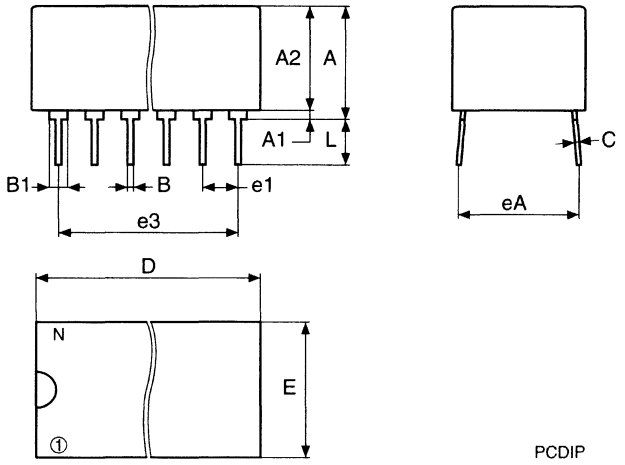
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP28 - 28 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

PCDIP28

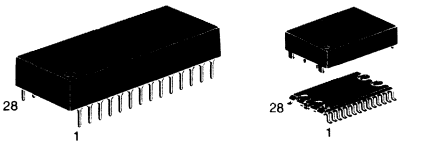


PCDIP

Drawing is not to scale

CMOS 8K x 8 ZEROPOWER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z58: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z58Y: 4.2V ≤ V_{PFD} ≤ 4.5V
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY
- SNAPHAT HOUSING (BATTERY) REPLACEABLE
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 8K x 8 SRAMs



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

DESCRIPTION

The M48Z58 ZEROPOWER® RAM is an 8K x 8 non-volatile static RAM that integrates power-fail deselect circuitry and battery control logic on a single die. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory solution.

Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

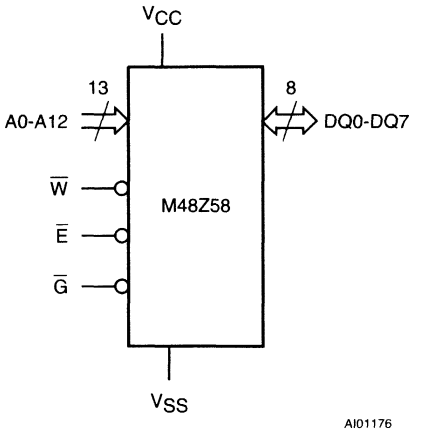
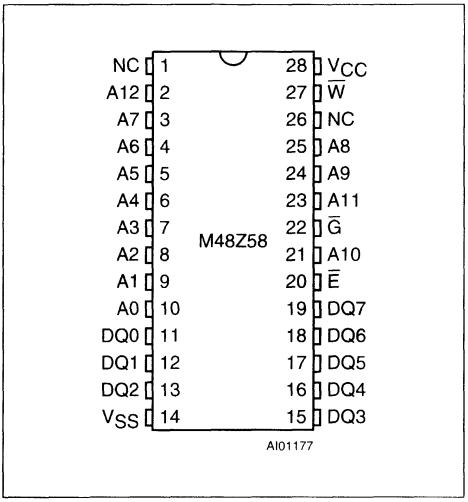
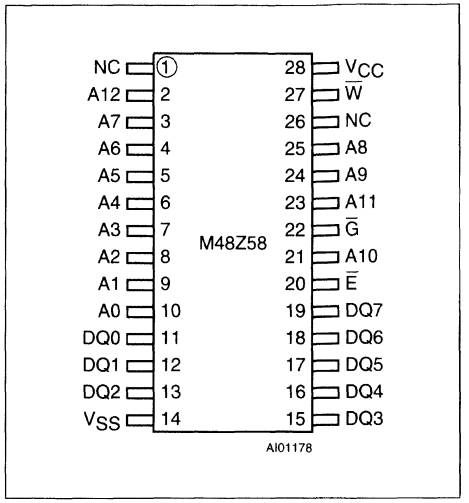


Figure 2A. DIP Pin Connections



Warning: NC = Not Connected

Figure 2B. SO Pin Connections



Warning: NC = Not Connected

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

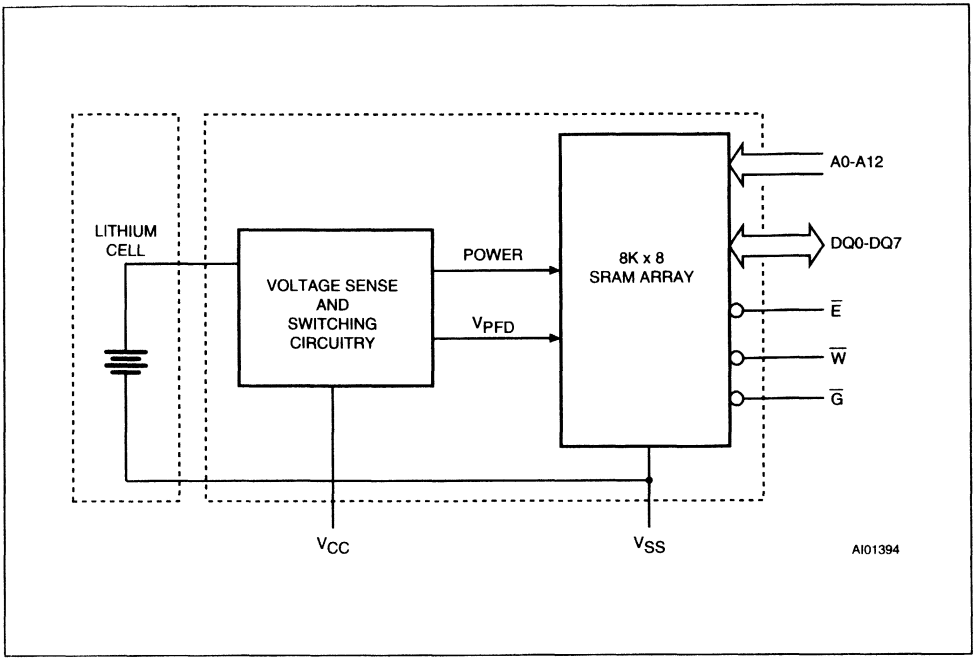
Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes (1)

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min) (2)	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	High Z	Battery Back-up Mode

Notes: 1. X = V_{IH} or V_{IL}
2. See Table 6 for details.

Figure 3. Block Diagram



DESCRIPTION (cont'd)

The M48Z58 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 28 pin 600mil DIP CAPHAT™ houses the M48Z58 silicon with a long life lithium button cell in a single package.

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

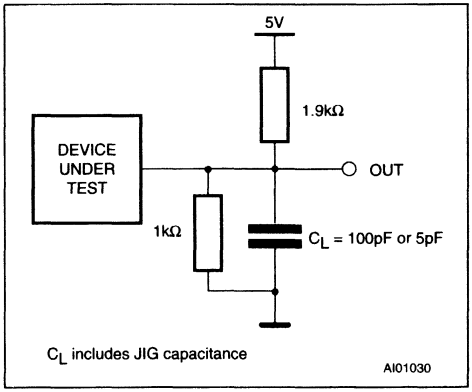


Table 4. Capacitance [1, 2] (T_A = 25 °C)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [3]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected.

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ = V_{CC} – 0.2V		3	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z58)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z58Y)	4.2	4.35	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} [2]	Expected Data Retention Time	10			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25 °C

DESCRIPTION (cont'd)

For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4Z28-BR00SH1".

The M48Z58 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition.

When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data until valid power returns.

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	10		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	V_{PFD} (max) to Inputs Recognized	40	200	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

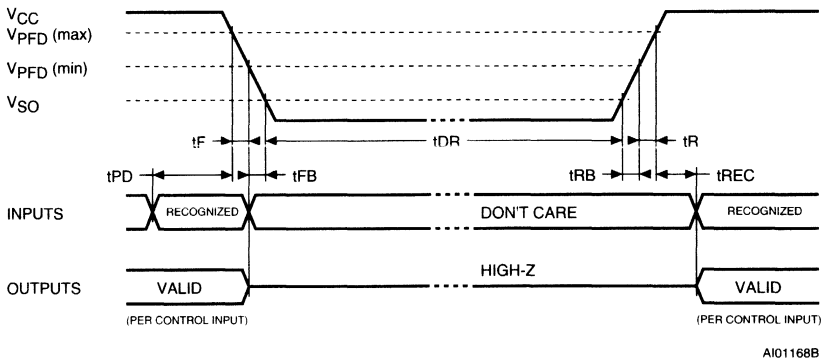
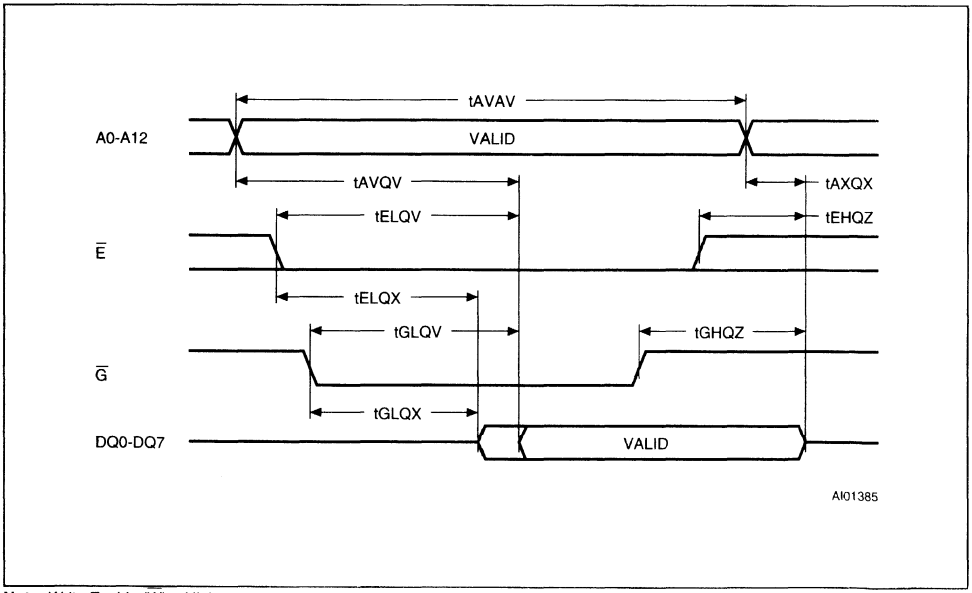


Table 8. Read Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z58 / 58Y		Unit
		-70		
		Min	Max	
t_{AVAV}	Read Cycle Time	70		ns
t_{AVQV} (1)	Address Valid to Output Valid		70	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		70	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		35	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		25	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		ns

Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4).

Figure 6. Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High.

Table 9. Write Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z58 / 58Y		Unit
		-70		
		Min	Max	
t_{AVAV}	Write Cycle Time	70		ns
t_{AVWL}	Address Valid to Write Enable Low	0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		ns
t_{WLWH}	Write Enable Pulse Width	50		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	55		ns
t_{WHAX}	Write Enable High to Address Transition	0		ns
t_{EHAX}	Chip Enable High to Address Transition	0		ns
t_{DVWH}	Input Valid to Write Enable High	30		ns
t_{DVEH}	Input Valid to Chip Enable High	30		ns
t_{WHDX}	Write Enable High to Input Transition	5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		ns
t_{WLQZ} (1, 2)	Write Enable Low to Output Hi-Z		25	ns
t_{AVWH}	Address Valid to Write Enable High	60		ns
t_{AVEH}	Address Valid to Chip Enable High	60		ns
t_{WHQX} (1, 2)	Write Enable High to Output Transition	5		ns

Notes: 1. C_L = 5pF (see Figure 4).
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

READ MODE

The M48Z58 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E}$ (Chip Enable) is low. Thus, the unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48Z58 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are low. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 7. Write Enable Controlled, Write AC Waveforms

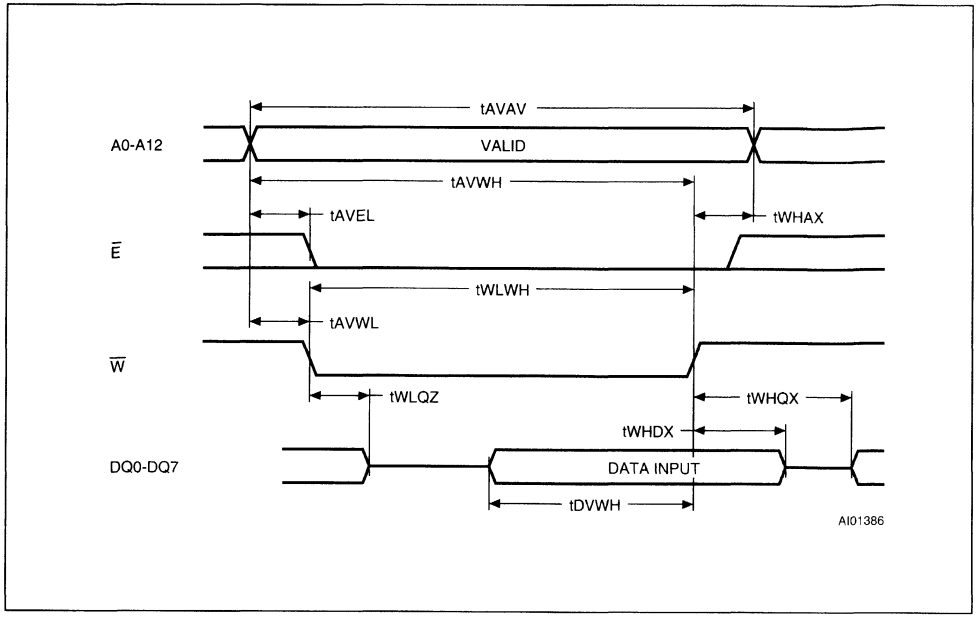
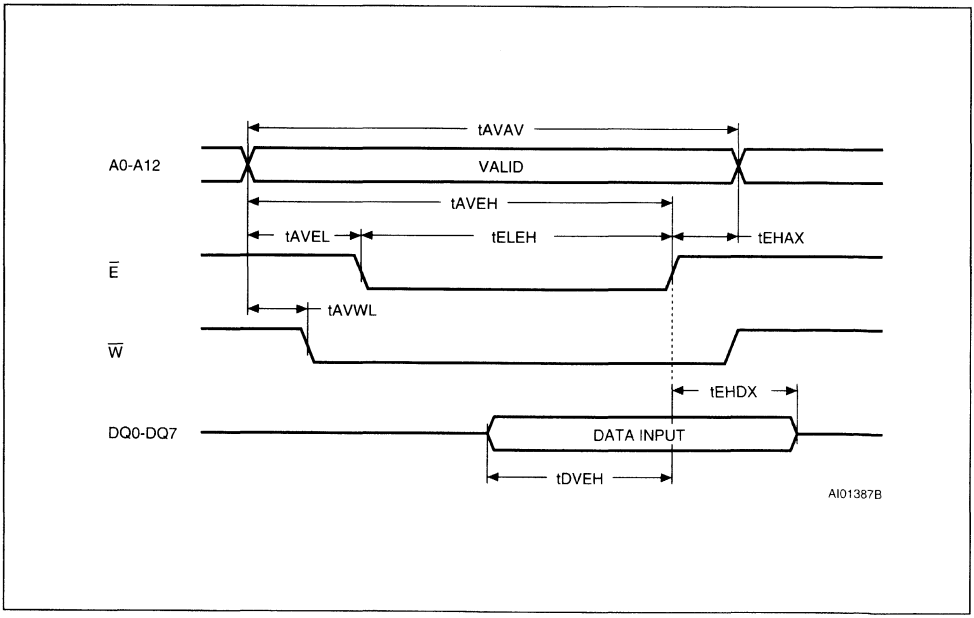


Figure 8. Chip Enable Controlled, Write AC Waveforms



DATA RETENTION MODE

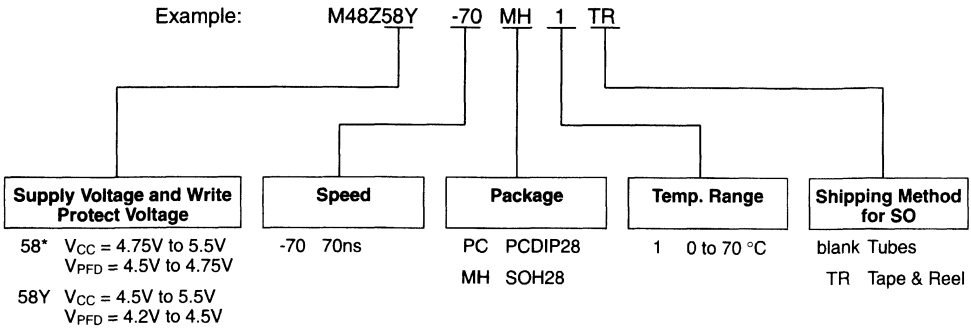
With valid V_{CC} applied, the M48Z58 operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z58 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data. The internal button cell will maintain data in the M48Z58 for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}.

As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues for t_{REC} until V_{CC} reaches V_{PFD}(min). Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max).

ORDERING INFORMATION SCHEME



Note: 58* CAPHAT package only.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4Z28-BR00SH1".

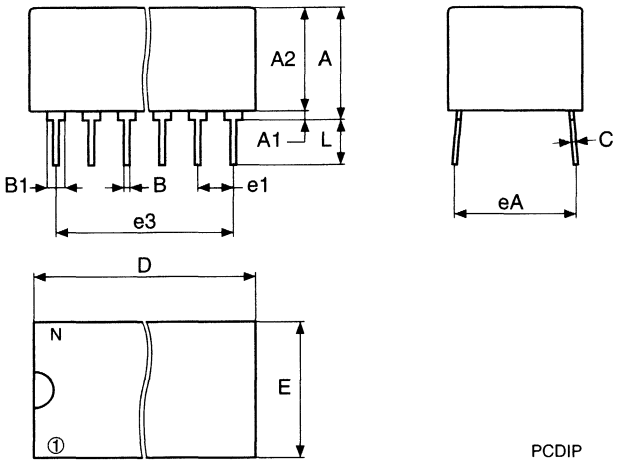
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP28 - 28 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

PCDIP28



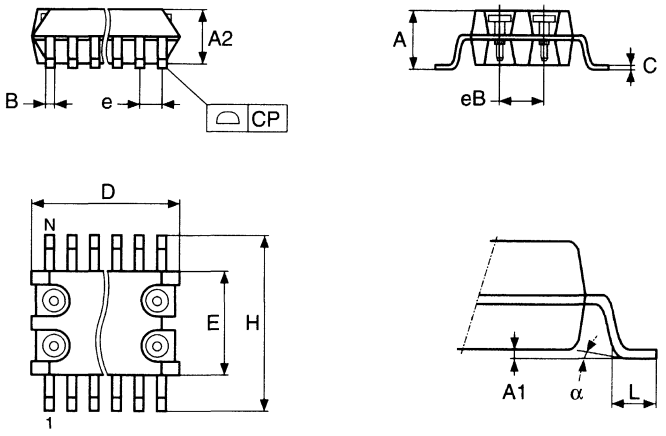
PCDIP

Drawing is not to scale

SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SOH28



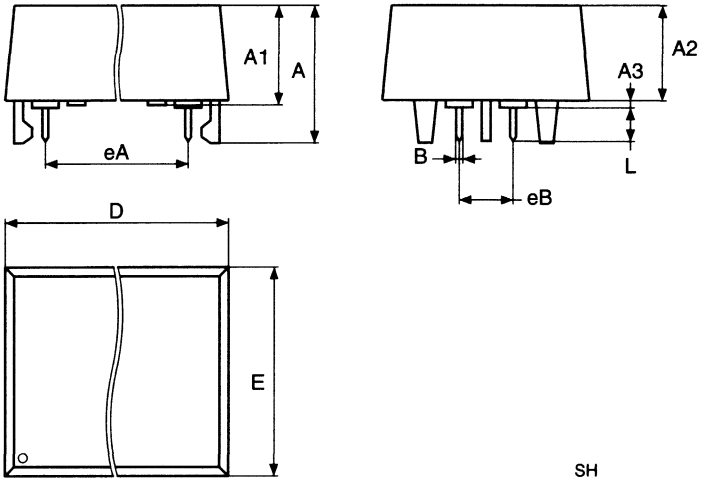
SOH

Drawing is not to scale

SH28 - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

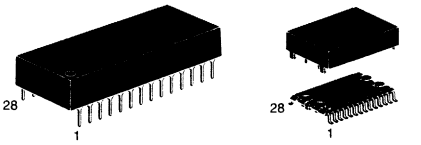
SH28



Drawing is not to scale

CMOS 8K x 8 ZEROPOWER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- MICROPROCESSOR POWER-ON RESET (Valid all the way to $V_{CC} = V_{SS}$)
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z59: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z59Y: 4.2V ≤ V_{PFD} ≤ 4.5V
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY
- SNAPHAT HOUSING (BATTERY) REPLACEABLE
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 8K x 8 SRAMs



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

DESCRIPTION

The M48Z59 ZEROPOWER® RAM is an 8K x 8 non-volatile static RAM that integrates power-fail deselect circuitry and battery control logic on a single die. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory solution.

Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{RST}$	Power Fail Reset Ouput (Open Drain)
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

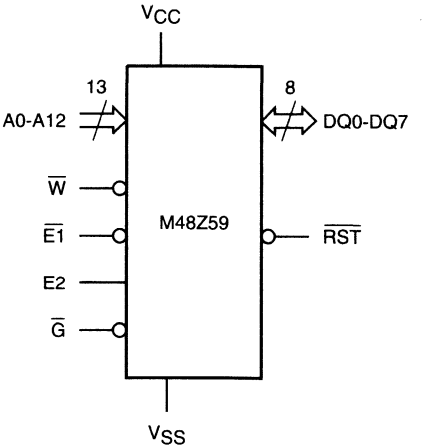


Figure 2A. DIP Pin Connections

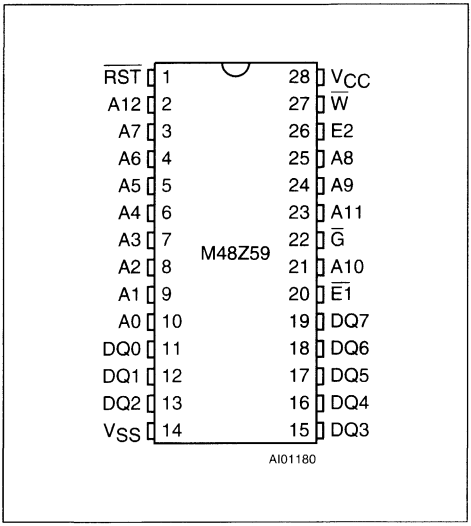


Figure 2B. SO Pin Connections

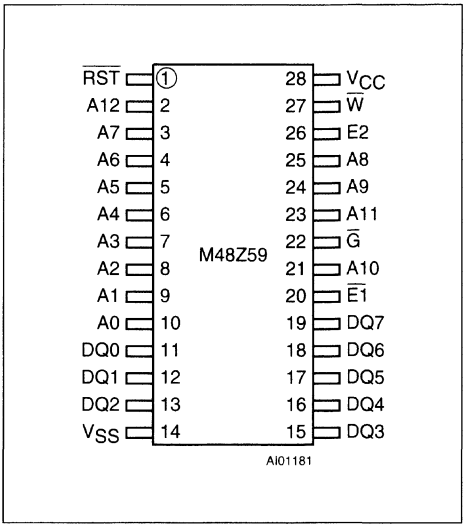


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

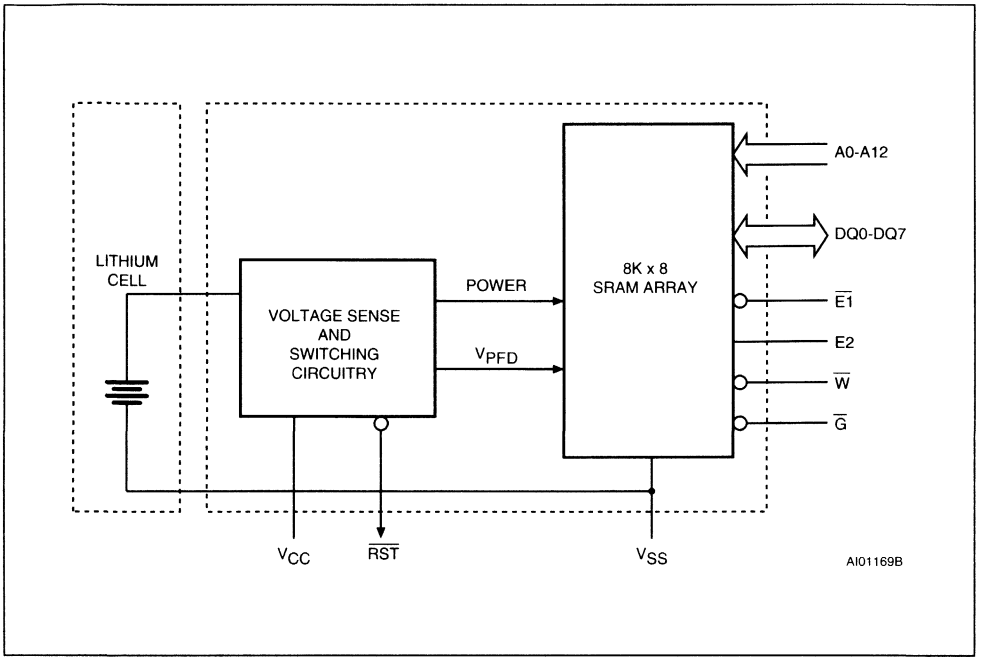
Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes (1)

Mode	V_{CC}	$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	X	High Z	Standby
Deselect		X	V_{IL}	X	X	High Z	Standby
Write		V_{IL}	V_{IH}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min) (2)	X	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	X	High Z	Battery Back-up Mode

Note: 1. X = V_{IH} or V_{IL}
2. See Table 6 for details.

Figure 3. Block Diagram



DESCRIPTION (cont'd)

The M48Z59 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

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AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

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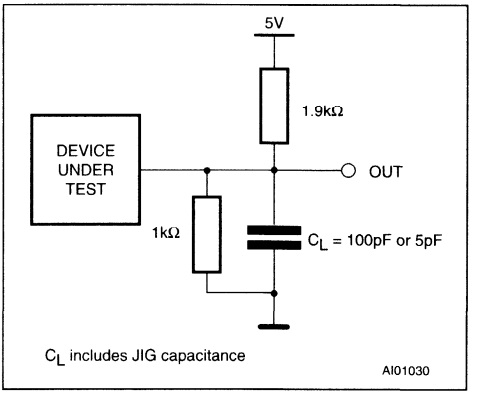

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Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} (1)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E1}$ = V_{IH}, E2 = V_{IL}		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E1}$ = V_{CC} – 0.2V, E2 = V_{SS} + 0.2V		3	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
	Output Low Voltage ($\overline{RST}$) (2)	I_{OL} = 10mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Notes: 1. Outputs Deselected.
2. The $\overline{RST}$ pin is Open Drain.

Table 6. Power Down/Up Trip Points DC Characteristics (1) (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z59)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z59Y)	4.2	4.35	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} (2)	Expected Data Retention Time	10			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25 °C.

DESCRIPTION (cont'd)

For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4Z28-BR00SH1".

A power-on reset output provides a reset pulse to the microprocessor. The reset pulls low (open drain) an power-down and remains low on power-up for 40ms to 200ms after V_{CC} passes V_{PFD}. The M48Z59 also has its own Power-fail Detect circuit.

The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data until valid power returns.

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E1}$ or $\overline{W}$ at V_{IH} or E2 at V_{IL} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	10		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	V_{PFD}(max) to $\overline{RST}$ High	40	200	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

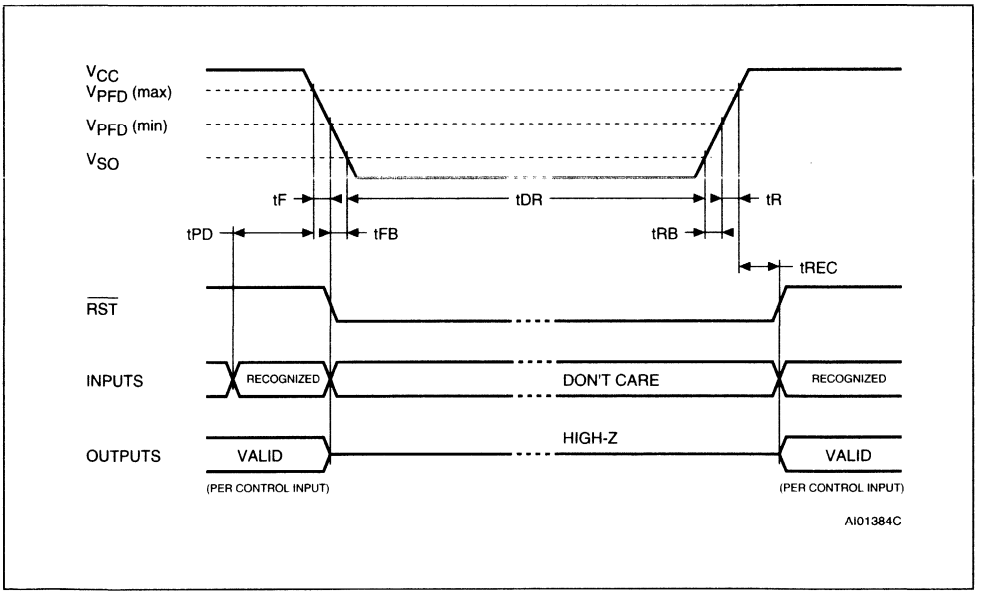
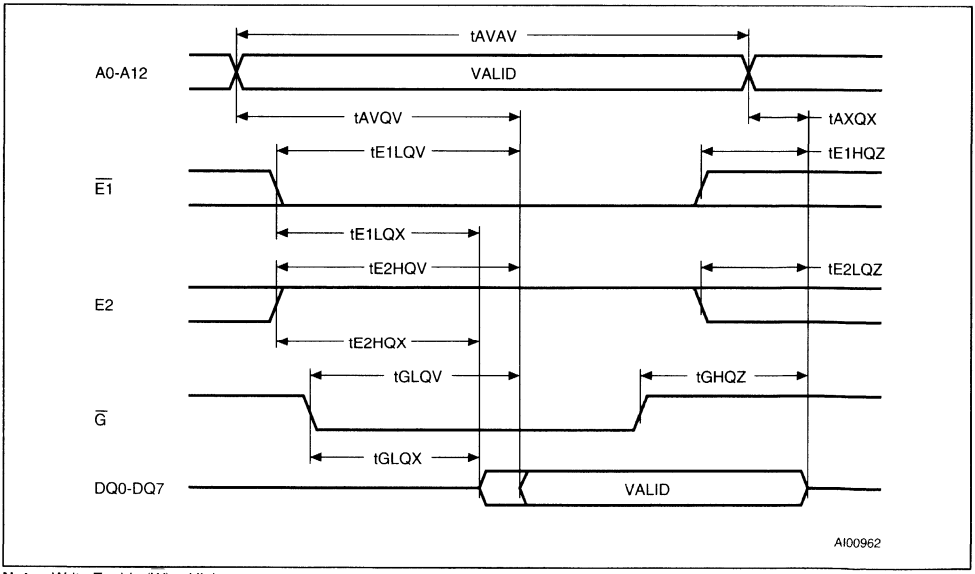


Table 8. Read Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z59 / 59Y		Unit
		-70		
		Min	Max	
t_{AVAV}	Read Cycle Time	70		ns
t_{AVQV} (1)	Address Valid to Output Valid		70	ns
t_{E1LQV} (1)	Chip Enable 1 Low to Output Valid		70	ns
t_{E2HQV} (1)	Chip Enable 2 High to Output Valid		70	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		35	ns
t_{E1LQX} (2)	Chip Enable 1 Low to Output Transition	5		ns
t_{E2HQX} (2)	Chip Enable 2 High to Output Transition	5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		ns
t_{E1HQZ} (2)	Chip Enable 1 High to Output Hi-Z		25	ns
t_{E2LQZ} (2)	Chip Enable 2 Low to Output Hi-Z		25	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		ns

Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4).

Figure 6. Read Mode AC Waveforms



Note: Write Enable (W) = High.

Table 9. Write Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z59 / 59Y		Unit
		-70		
		Min	Max	
t_{AVAV}	Write Cycle Time	70		ns
t_{AVWL}	Address Valid to Write Enable Low	0		ns
t_{AVE1L}	Address Valid to Chip Enable 1 Low	0		ns
t_{AVE2H}	Address Valid to Chip Enable 2 High	0		ns
t_{WLWH}	Write Enable Pulse Width	50		ns
t_{E1LE1H}	Chip Enable 1 Low to Chip Enable 1 High	55		ns
t_{E2HE2L}	Chip Enable 2 High to Chip Enable 2 Low	55		ns
t_{WHAX}	Write Enable High to Address Transition	0		ns
t_{E1HAX}	Chip Enable 1 High to Address Transition	0		ns
t_{E2LAX}	Chip Enable 2 Low to Address Transition	0		ns
t_{DVWH}	Input Valid to Write Enable High	30		ns
t_{DVE1H}	Input Valid to Chip Enable 1 High	30		ns
t_{DVE2L}	Input Valid to Chip Enable 2 Low	30		ns
t_{WHDX}	Write Enable High to Input Transition	5		ns
t_{E1HDX}	Chip Enable 1 High to Input Transition	5		ns
t_{E2LDX}	Chip Enable 2 Low to Input Transition	5		ns
t_{WLQZ} (1, 2)	Write Enable Low to Output Hi-Z		25	ns
t_{AVWH}	Address Valid to Write Enable High	60		ns
t_{AVE1H}	Address Valid to Chip Enable 1 High	60		ns
t_{AVE2L}	Address Valid to Chip Enable 2 Low	60		ns
t_{WHQX} (1, 2)	Write Enable High to Output Transition	5		ns

Notes: 1. C_L = 5pF (see Figure 4).
2. If E1 goes low or E2 high simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

Figure 7. Write Enable Controlled, Write AC Waveforms

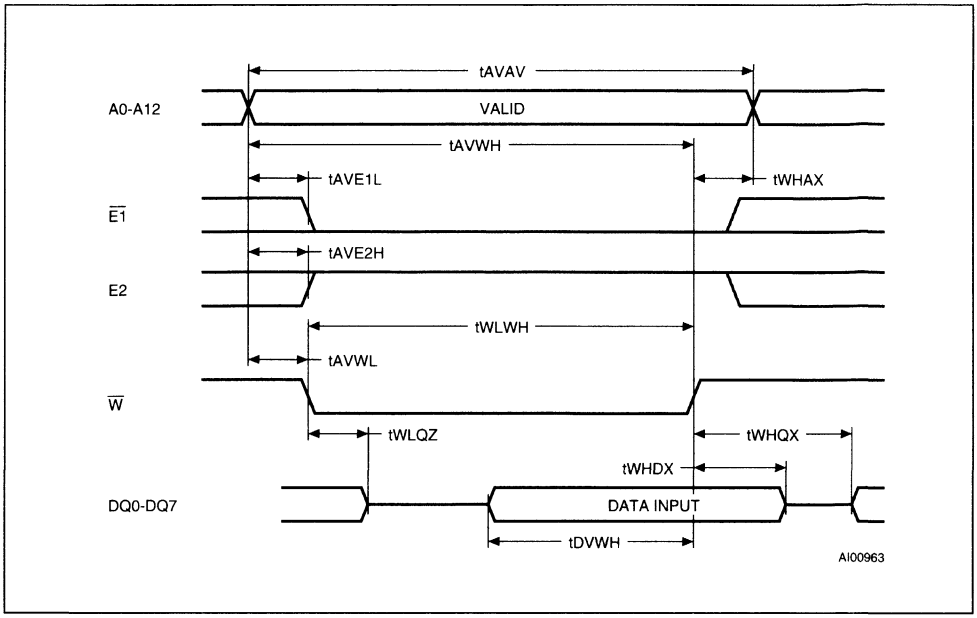
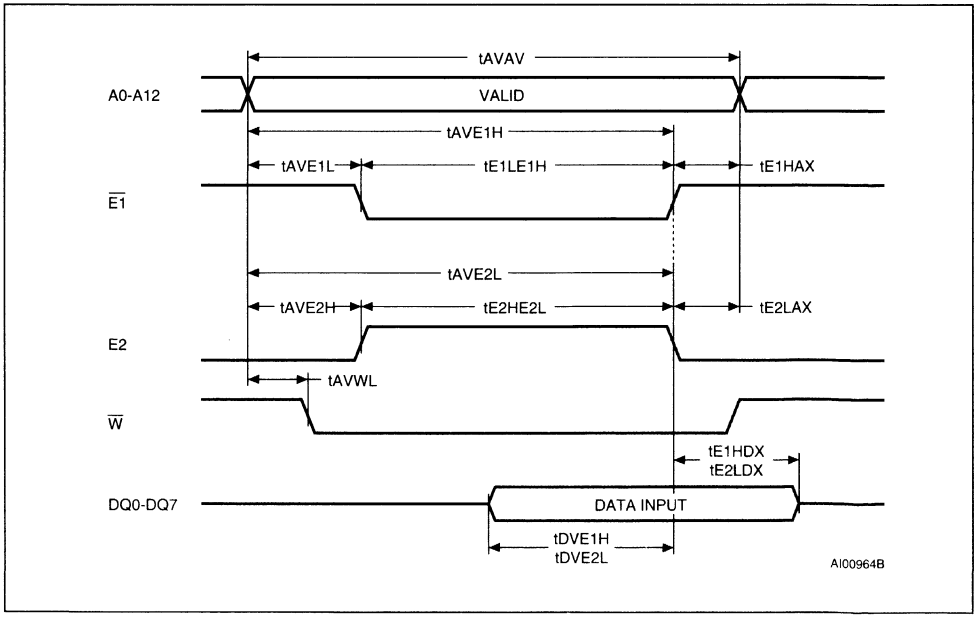


Figure 8. Chip Enable Controlled, Write AC Waveforms



READ MODE

The M48Z59 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E1}$ (Chip Enable 1) is low, and E2 (Chip Enable 2) is high. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E1}$, E2, and $\overline{G}$ access times are also satisfied. If the $\overline{E1}$, E2 and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Times (t_{E1LQV} or t_{E2HQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E1}$, E2 and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E1}$, E2 and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48Z59 is in the Write Mode whenever $\overline{W}$ and $\overline{E1}$ are low and E2 is high. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E1}$, or the rising edge of E2. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E1}$, or the falling edge of E2. The addresses must be held valid throughout the cycle. $\overline{E1}$ or $\overline{W}$ must return high or E2 low for minimum of t_{E1HAX} or t_{E2LAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E1}$ and $\overline{G}$ and a high on E2, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48Z59 operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

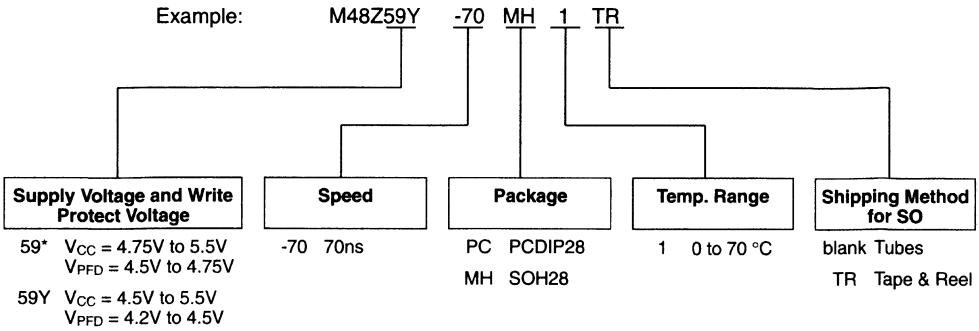
Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z59 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data. The internal button cell will maintain data in the M48Z59 for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues for t_{REC} until V_{CC} reaches V_{PFD}(min). $\overline{E1}$ should be kept high or E2 low as V_{CC} rises past V_{PFD}(min) to prevent inadvertent write cycles prior to processor stabilization. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max).

POWER-ON RESET

The M48Z59 continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ pulls low (open drain) and remains low on power-up for 40ms to 200ms after V_{CC} passes V_{PFD}. A 1kΩ resistor is recommended in order to control the rise-time. The reset pulse remains active with V_{CC} at V_{SS}.

ORDERING INFORMATION SCHEME



Note: 59* CAPHAT package only.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4Z28-BR00SH1".

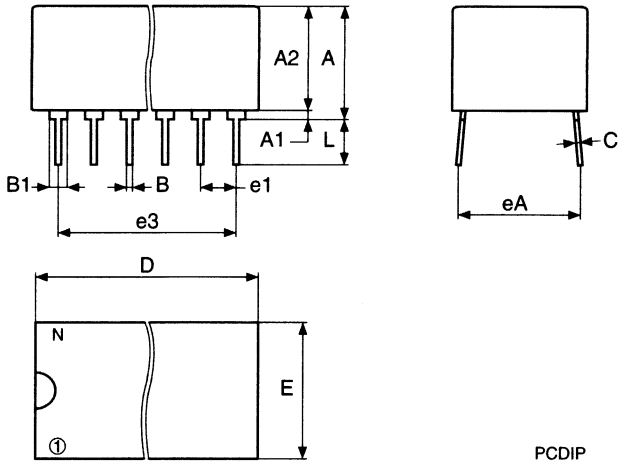
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP28 - 28 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

PCDIP28



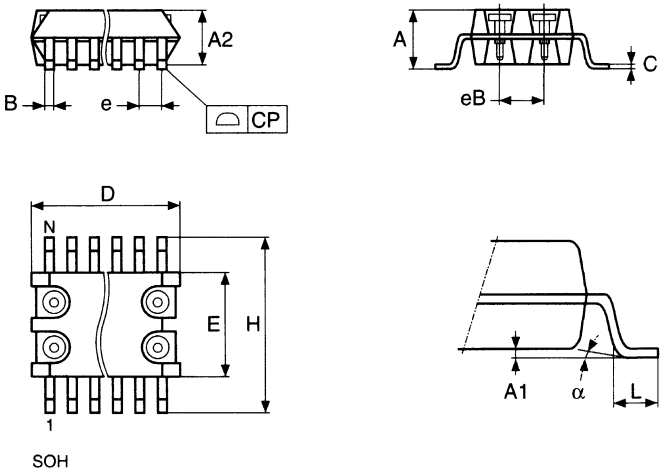
PCDIP

Drawing is not to scale

SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SOH28



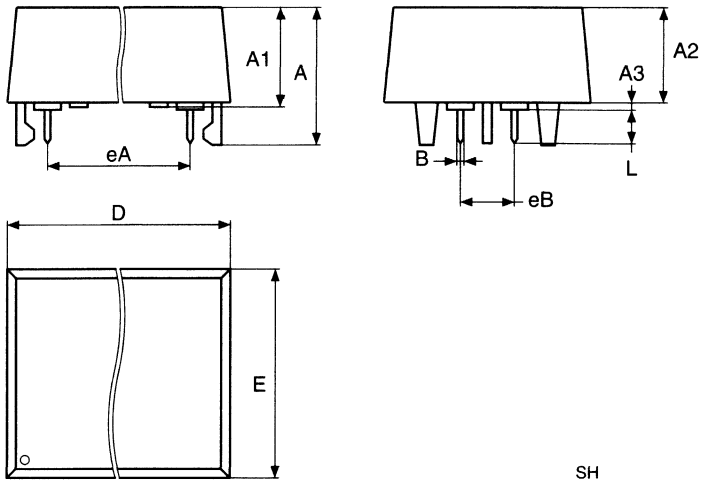
SOH

Drawing is not to scale

SH28 - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

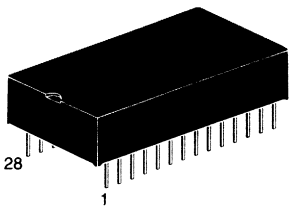
SH28



Drawing is not to scale

CMOS 32K x 8 ZEROPOWER SRAM

- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 32K x 8 SRAMs
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z30: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z30Y: 4.2V ≤ V_{PFD} ≤ 4.50V
- BATTERY INTERNALLY ISOLATED UNTIL POWER IS APPLIED



PMDIP28 (PM)
Module

DESCRIPTION

The M48Z30/30Y 32K x 8 ZEROPOWER® RAM is a non-volatile 262,144 bit Static RAM organized as 32,768 words by 8 bits. The device combines an internal lithium battery and a full CMOS SRAM in a plastic 28 pin DIP Module. The ZEROPOWER

Table 1. Signal Names

A0 - A14	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

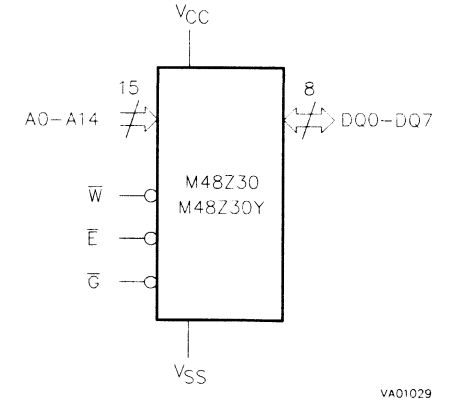


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 70	°C
T_{BIAS}	Temperature Under Bias	–10 to 70	°C
T_{SLD}	Lead Soldering Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

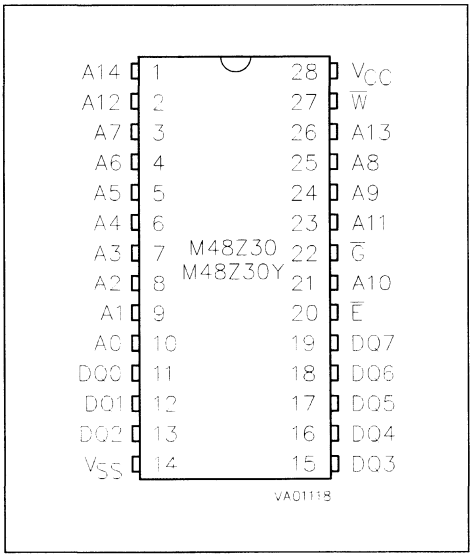
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

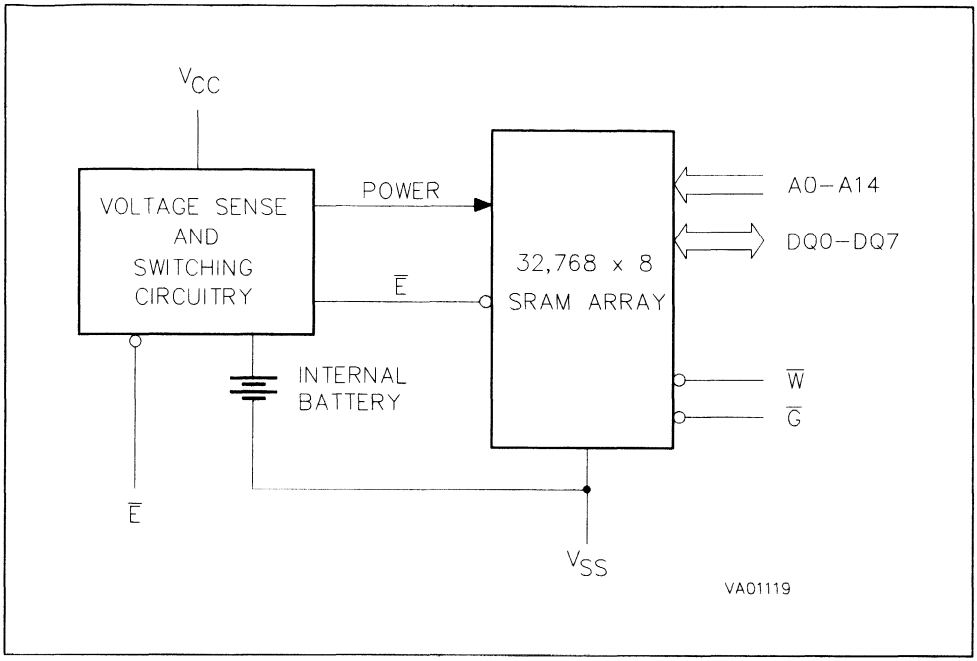
RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z30/30Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which sustains data until valid power returns.

READ MODE

The M48Z30/30Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address

Figure 3. Block Diagram



specified by the 15 Address Inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48Z30/30Y is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

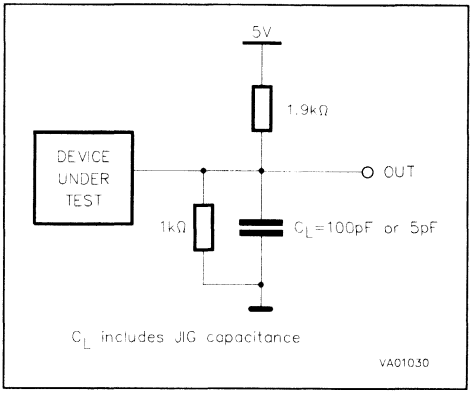


Table 4. Capacitance [1, 2] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [3]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO} [1]	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, Outputs open		85	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		7	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} \ge V_{CC} - 0.2V$		4	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs deselected.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z30)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z30Y)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3		V
t_{DR} [2]	Data Retention Time	10			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_{WP}	Write Protect Time from V_{CC} = V_{PFD}	40	150	µs
t_R	V_{SO} to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{ER}	$\overline{E}$ Recovery Time	40	120	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).

2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

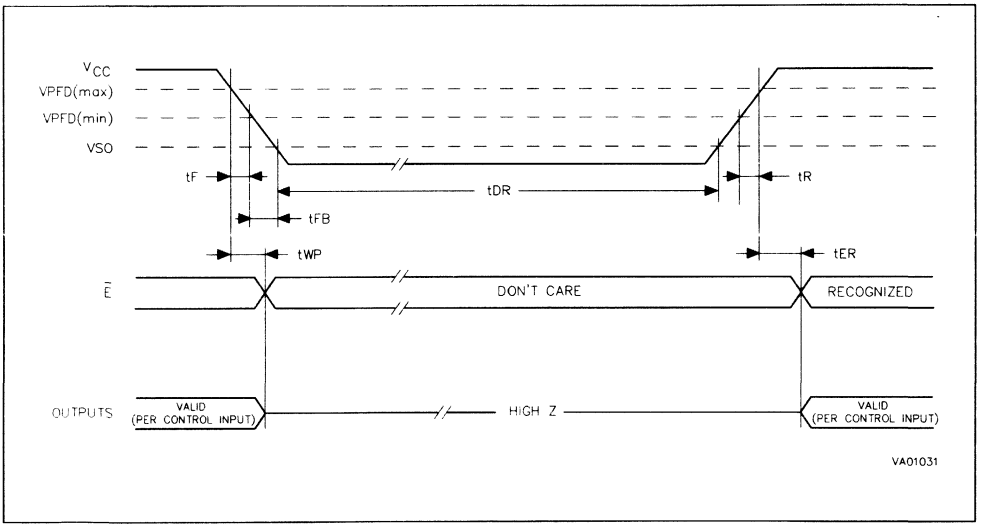
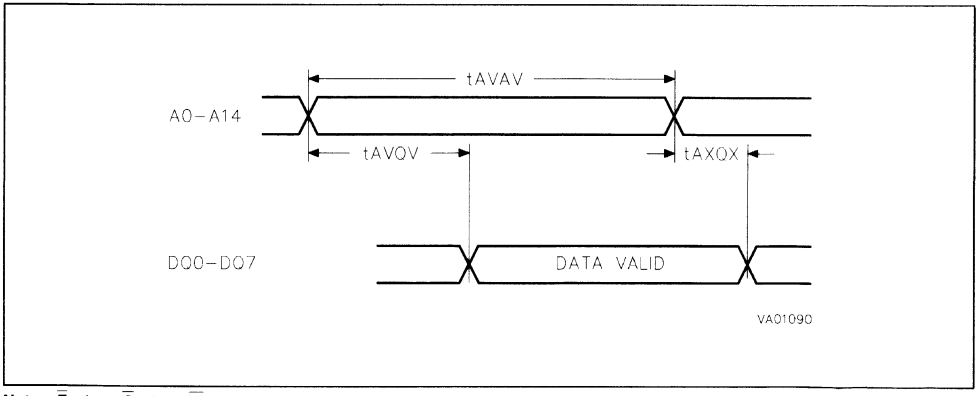


Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z30 / 30Y				Unit
		-85		-100		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	85		100		ns
t_{AVQV} (1)	Address Valid to Output Valid		85		100	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		85		100	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		45		50	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		5		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		40		40	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		35		35	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		10		ns

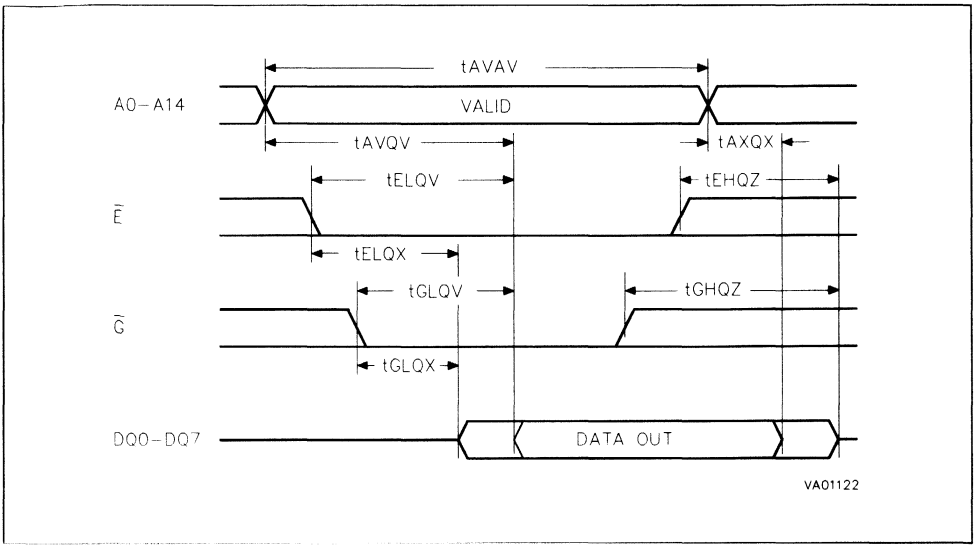
Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4)

Figure 6. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{W}$ = High.

Figure 7. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: $\overline{W}$ = High.

WRITE MODE (cont'd)

A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} or t_{EHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48Z30/30Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data.

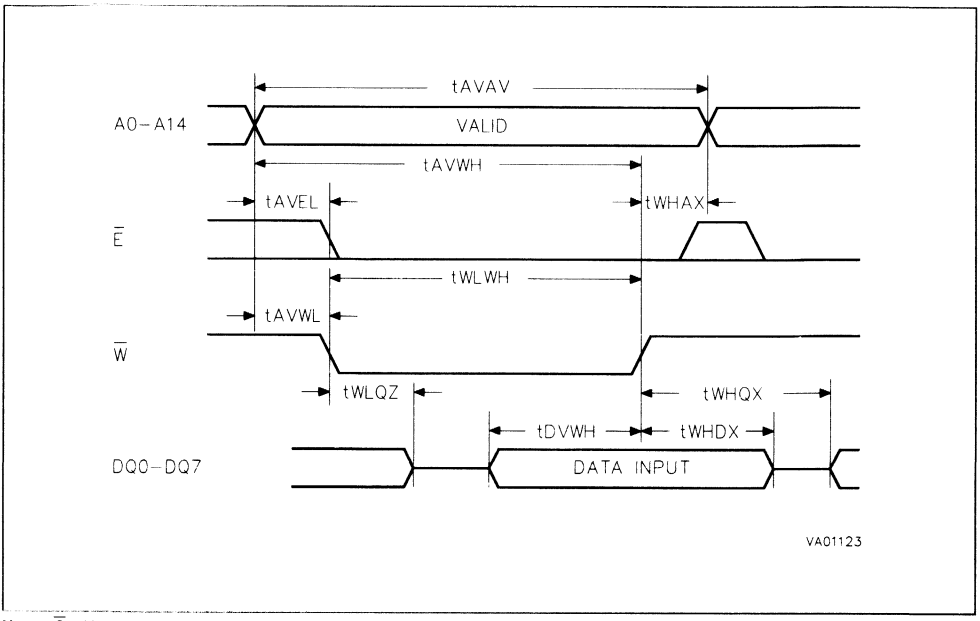
The internal coin cell will maintain data in the M48Z30/30Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the battery is disconnected, and the power supply is switched to external Vcc. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z30 / 30Y				Unit
		-85		-100		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	85		100		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{WLWH}	Write Enable Pulse Width	65		75		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	75		90		ns
t_{WHAX}	Write Enable High to Address Transition	5		5		ns
t_{EHAX}	Chip Enable High to Address Transition	15		15		ns
t_{DVWH}	Input Valid to Write Enable High	35		40		ns
t_{DVEH}	Input Valid to Chip Enable High	35		40		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	15		15		ns
t_{WLQZ} (1,2)	Write Enable Low to Output Hi-Z		35		35	ns
t_{AVWH}	Address Valid to Write Enable High	75		80		ns
t_{AVEH}	Address Valid to Chip Enable High	75		80		ns
t_{WHQX} (1,2)	Write Enable High to Output Transition	5		5		ns

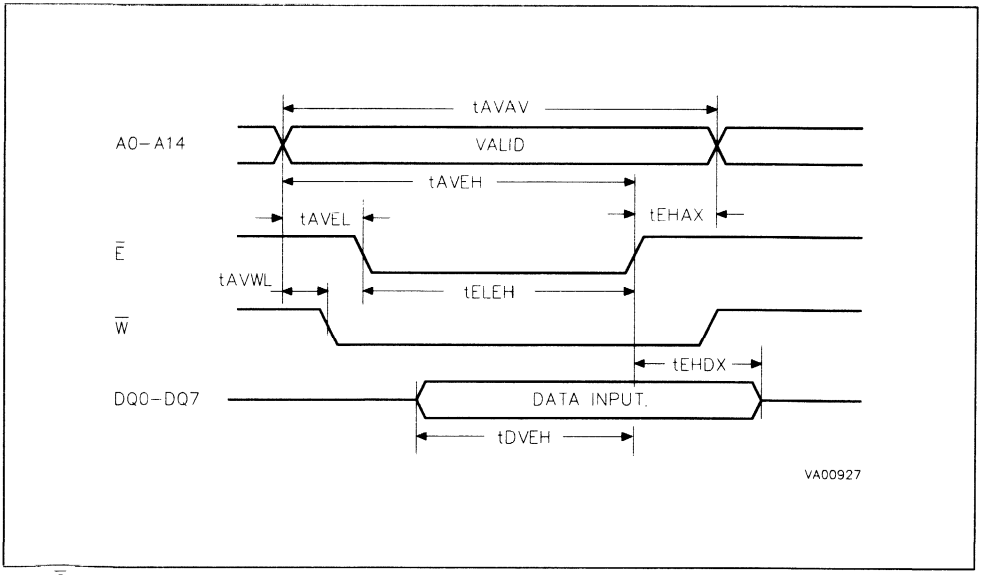
Notes: 1. C_L = 5pF (see Figure 4).
2. If E goes low simultaneously with $\overline{W}$ going low after $\overline{W}$ going low, the outputs remain in the high-impedance state.

Figure 8. Write Enable Controlled, Write AC Waveforms



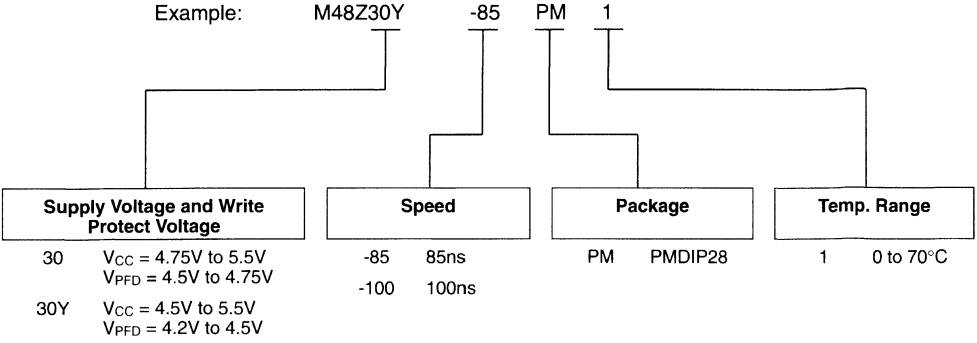
Note: $\overline{G}$ = High.

Figure 9. Chip Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = High.

ORDERING INFORMATION SCHEME



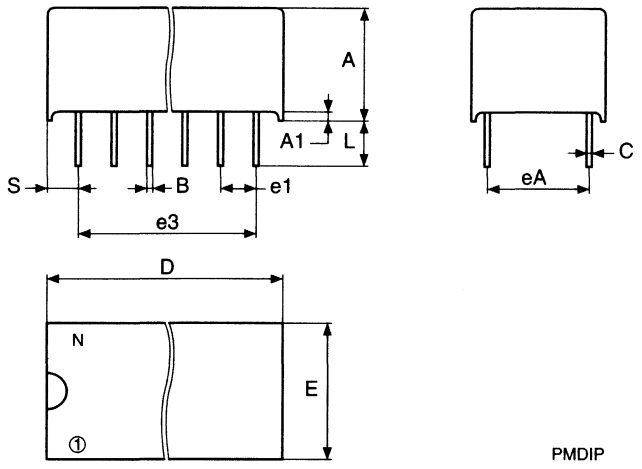
For a list of available options (Package and Speed) refer to the current Memory Shortform catalogue.

For further information or any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PMDIP28 - 28 pin Plastic DIP Module

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		9.27	9.52		0.365	0.375
A1		0.38	–		0.015	–
B		0.43	0.59		0.017	0.023
C		0.20	0.33		0.008	0.013
D		37.34	38.10		1.470	1.500
E		18.03	18.80		0.710	0.740
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		14.99	16.00		0.590	0.630
L		3.05	3.81		0.120	0.150
S		1.91	2.79		0.075	0.110
N	28			28		

PMDIP28



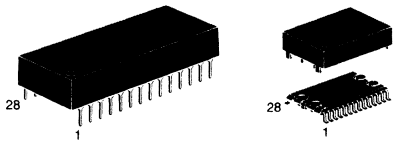
PMDIP

Drawing is not to scale

CMOS 32K x 8 ZEROPOWER SRAM

PRELIMINARY DATA

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z35: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z35Y: 4.2V ≤ V_{PFD} ≤ 4.5V
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY
- SNAPHAT HOUSING (BATTERY) REPLACEABLE
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 32K x 8 SRAMs



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

DESCRIPTION

The M48Z35 ZEROPOWER® RAM is an 32K x 8 non-volatile static RAM that integrates power-fail deselect circuitry and battery control logic on a single die. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory solution.

Table 1. Signal Names

A0-A14	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

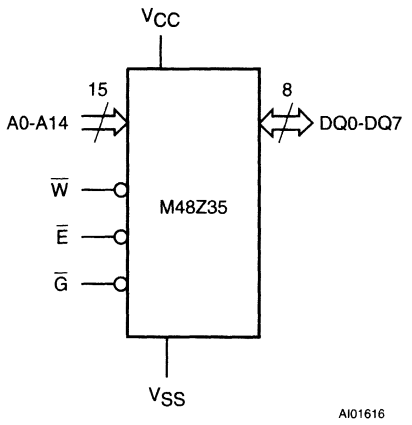


Figure 2A. DIP Pin Connections

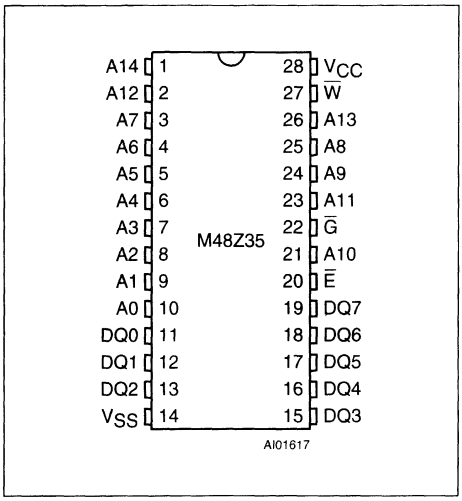


Figure 2B. SO Pin Connections

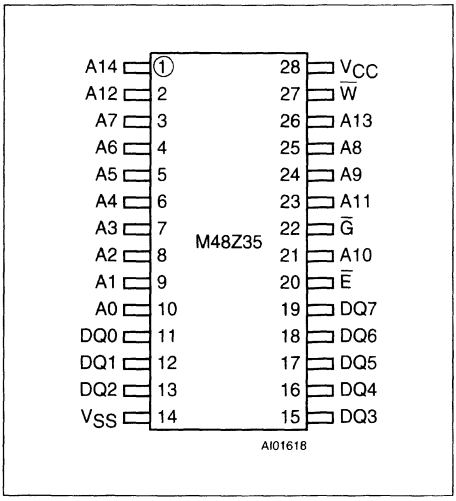


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

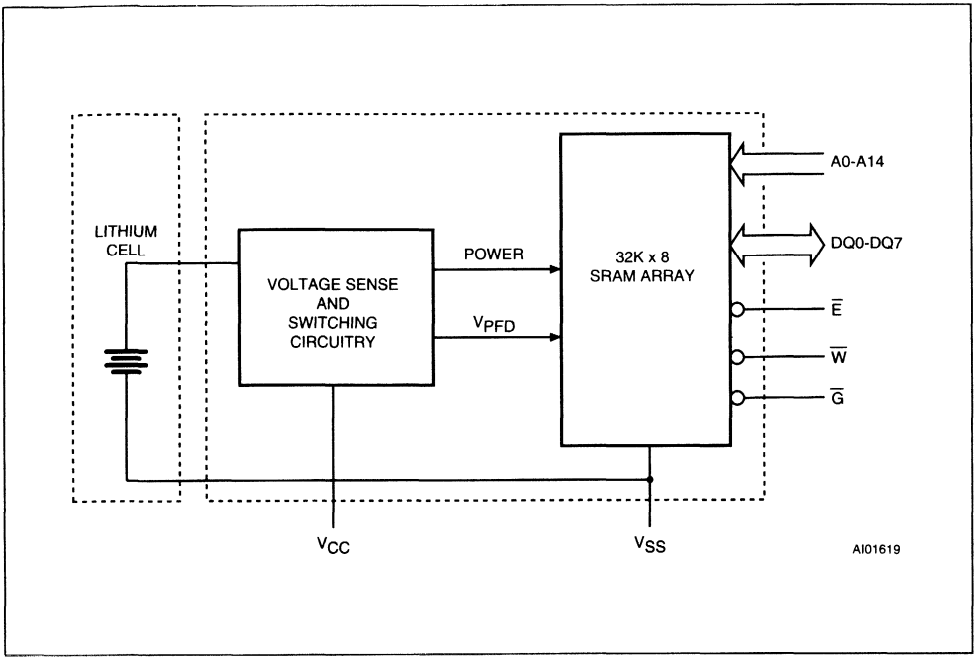
Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes (1)

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min) (2)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	High Z	Battery Back-up Mode

Notes: 1. X = V_{IH} or V_{IL}
2. See Table 6 for details.

Figure 3. Block Diagram



DESCRIPTION (cont'd)

The M48Z35 is a non-volatile pin and function equivalent to any JEDEC standard 32K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 28 pin 600mil DIP CAPHAT™ houses the M48Z35 silicon with a long life lithium button cell in a single package.

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

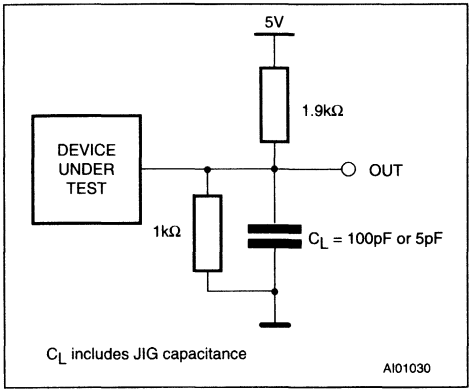


Table 4. Capacitance [1, 2] (T_A = 25 °C)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [3]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected.

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ = V_{CC} – 0.2V		3	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z35)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z35Y)	4.2	4.35	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} [2]	Expected Data Retention Time	10			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25 °C

DESCRIPTION (cont'd)

For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4Z28-BR00SH1".

The M48Z35 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition.

When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data until valid power returns.

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	10		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	V_{PFD} (max) to Inputs Recognized	40	200	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

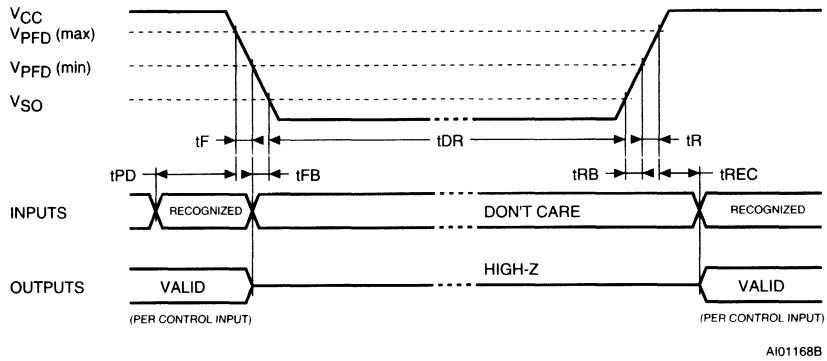
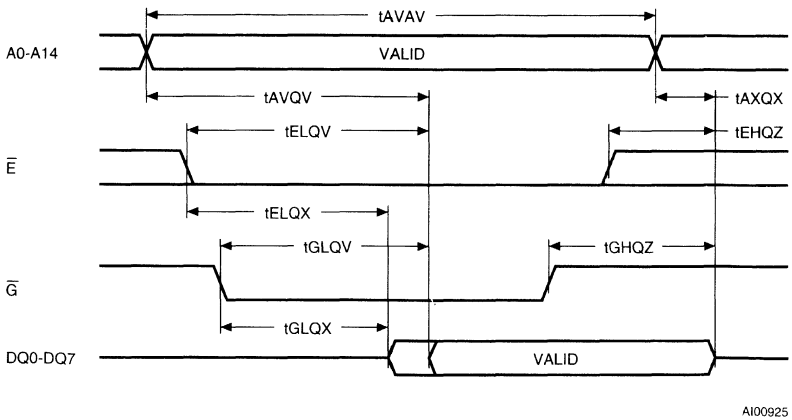


Table 8. Read Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z35 / 35Y		Unit
		-70		
		Min	Max	
t_{AVAV}	Read Cycle Time	70		ns
t_{AVQV} (1)	Address Valid to Output Valid		70	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		70	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		35	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		25	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		ns

Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4).

Figure 6. Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High.

Table 9. Write Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z35 / 35Y		Unit
		-70		
		Min	Max	
t_{AVAV}	Write Cycle Time	70		ns
t_{AVWL}	Address Valid to Write Enable Low	0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		ns
t_{WLWH}	Write Enable Pulse Width	50		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	55		ns
t_{WHAX}	Write Enable High to Address Transition	0		ns
t_{EHAX}	Chip Enable High to Address Transition	0		ns
t_{DVWH}	Input Valid to Write Enable High	30		ns
t_{DVEH}	Input Valid to Chip Enable High	30		ns
t_{WHDX}	Write Enable High to Input Transition	5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		ns
t_{WLQZ} (1, 2)	Write Enable Low to Output Hi-Z		25	ns
t_{AVWH}	Address Valid to Write Enable High	60		ns
t_{AVEH}	Address Valid to Chip Enable High	60		ns
t_{WHQX} (1, 2)	Write Enable High to Output Transition	5		ns

Notes: 1. C_L = 5pF (see Figure 4).
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

READ MODE

The M48Z35 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 264,144 locations in the static storage array. Thus, the unique address specified by the 15 Address Inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48Z35 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are low. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of W or E. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 7. Write Enable Controlled, Write AC Waveforms

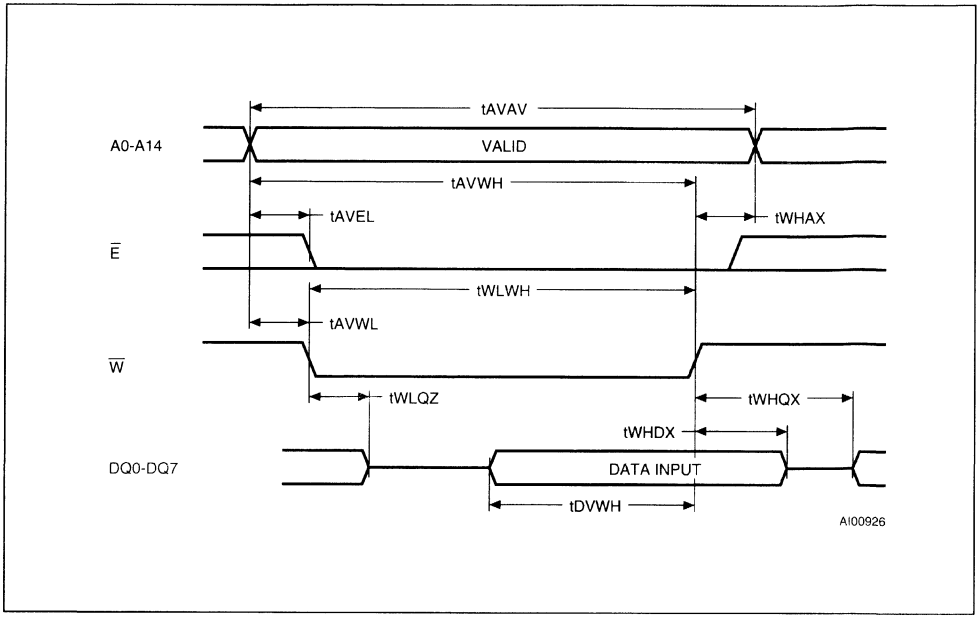
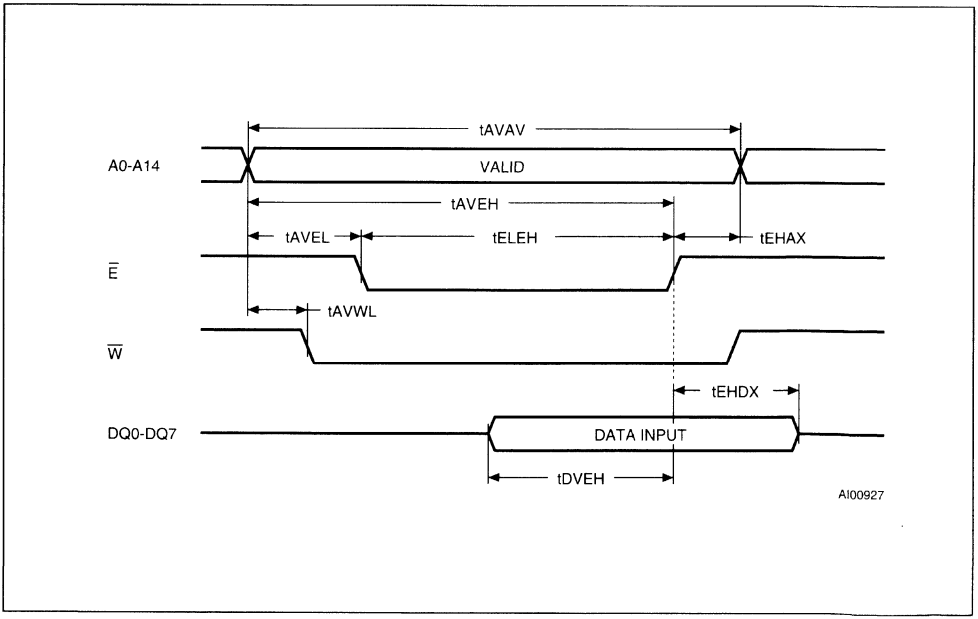


Figure 8. Chip Enable Controlled, Write AC Waveforms



DATA RETENTION MODE

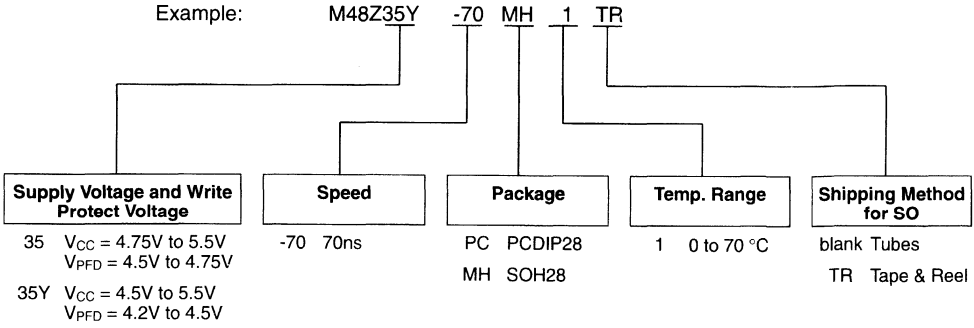
With valid V_{CC} applied, the M48Z35 operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z35 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data. The internal button cell will maintain data in the M48Z35 for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}.

As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues for t_{REC} until V_{CC} reaches V_{PFD}(min). Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max).

ORDERING INFORMATION SCHEME



The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4Z28-BR00SH1".

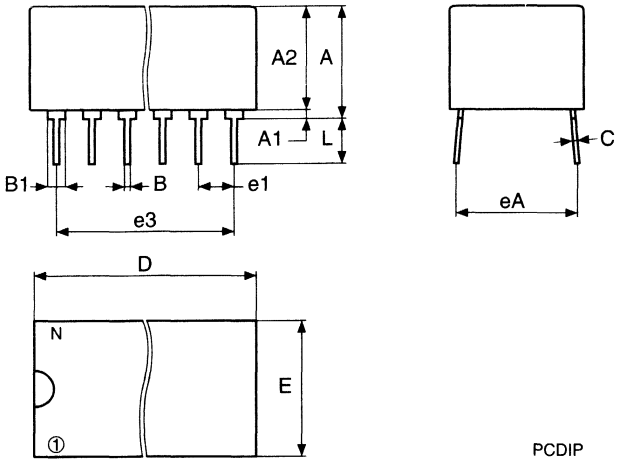
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP28 - 28 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

PCDIP28



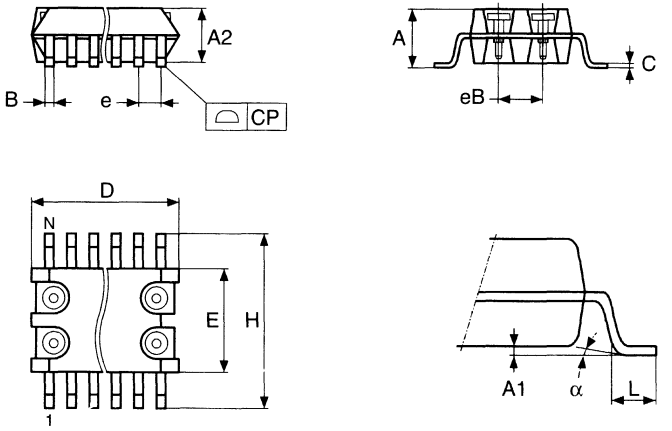
PCDIP

Drawing is not to scale

SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SOH28



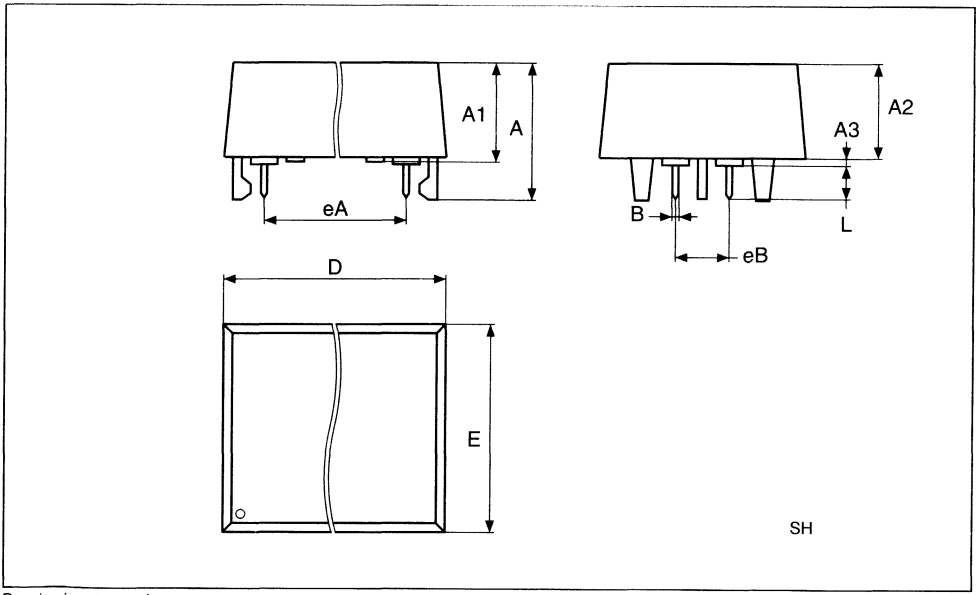
SOH

Drawing is not to scale

SH28 - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

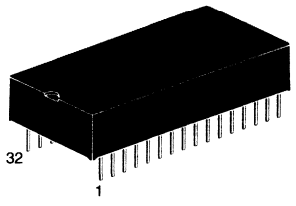
SH28



Drawing is not to scale

CMOS 128K x 8 ZEROPOWER SRAM

- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 128K x 8 SRAMs
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z128: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z128Y: 4.2V ≤ V_{PFD} ≤ 4.50V
- BATTERY INTERNALLY ISOLATED UNTIL POWER IS APPLIED



PMDIP32 (PM)
Module

DESCRIPTION

The M48Z128/128Y 128K x 8 ZEROPOWER® RAM is a non-volatile 1,048,576 bit Static RAM organized as 131,072 words by 8 bits. The device combines an internal lithium battery and a full CMOS SRAM in a plastic 32 pin DIP Module.

Table 1. Signal Names

A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

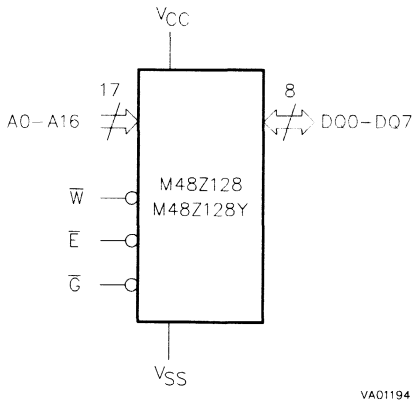


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 70	°C
T_{BIAS}	Temperature Under Bias	–10 to 70	°C
T_{SLD}	Lead Soldering Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

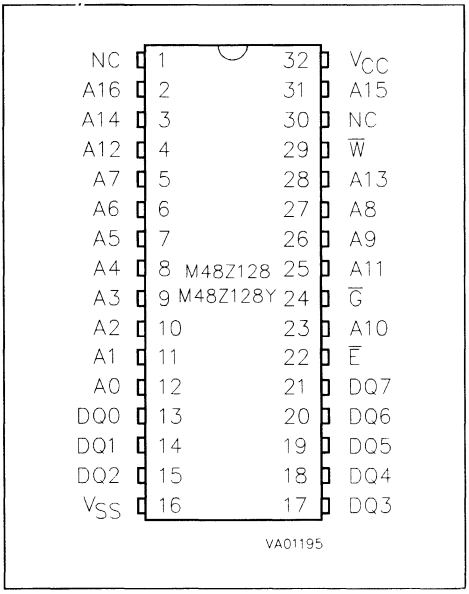
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

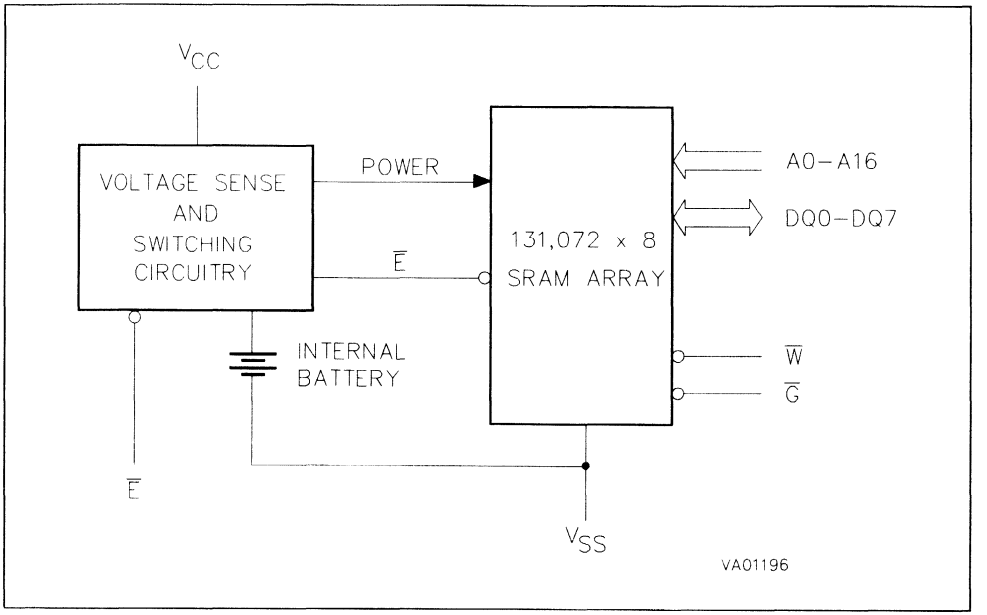
The ZEROPOWER RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z128/128Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which sustains data until valid power returns.

READ MODE

The M48Z128/128Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 1,048,576 locations in the static storage array. Thus, the unique address specified by the 17 Address Inputs defines which

Figure 3. Block Diagram



one of the 131,072 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48Z128/128Y is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

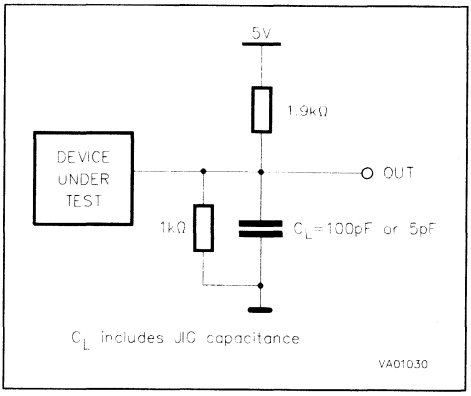


Table 4. Capacitance [1, 2] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [3]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} [1]	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±1	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, Outputs open		105	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		7	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ ≥ V_{CC} – 0.2V		4	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs deselected.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z128)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z128Y)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3		V
t_{DR} [2]	Data Retention Time	10			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_{WP}	Write Protect Time from V_{CC} = V_{PFD}	40	150	µs
t_R	V_{SO} to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{ER}	$\overline{E}$ Recovery Time	40	120	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

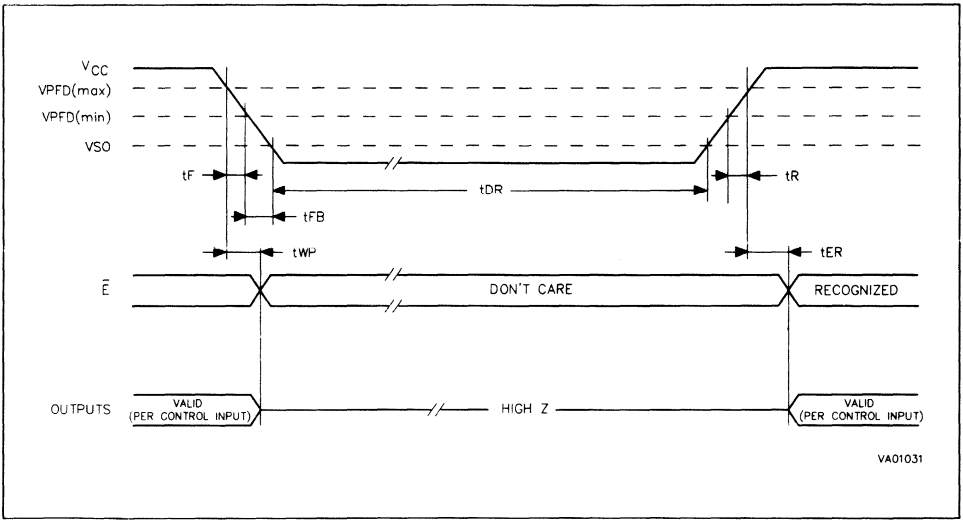
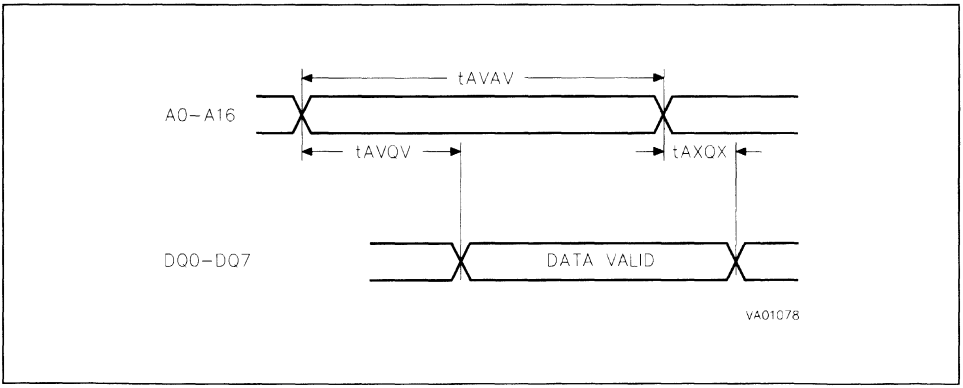


Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z128 / 128Y				Unit
		-85		-120		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	85		120		ns
t_{AVQV} (1)	Address Valid to Output Valid		85		120	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		85		120	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		45		60	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		35		45	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25		35	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		10		ns

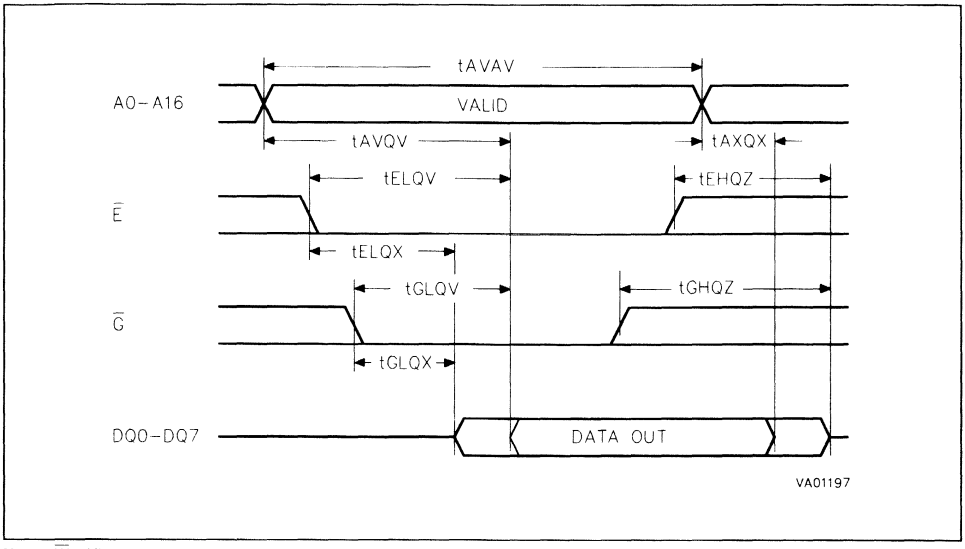
Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4)

Figure 6. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{W}$ = High.

Figure 7. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: $\overline{W}$ = High.

WRITE MODE (cont'd)

The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} or t_{EHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48Z128/128Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data.

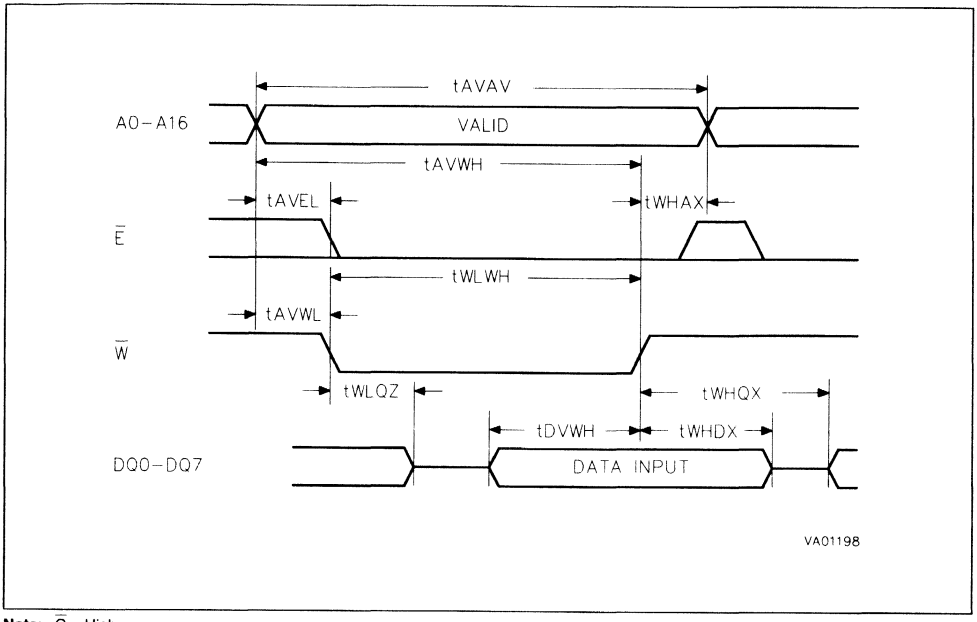
The internal coin cell will maintain data in the M48Z128/128Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the battery is disconnected, and the power supply is switched to external Vcc. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z128 / 128Y				Unit
		-85		-120		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	85		120		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{WLWH}	Write Enable Pulse Width	65		85		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	75		100		ns
t_{WHAX}	Write Enable High to Address Transition	5		5		ns
t_{EHAX}	Chip Enable High to Address Transition	15		15		ns
t_{DVWH}	Input Valid to Write Enable High	35		45		ns
t_{DVEH}	Input Valid to Chip Enable High	35		45		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	10		10		ns
t_{WLQZ} (1,2)	Write Enable Low to Output Hi-Z		30		40	ns
t_{AVWH}	Address Valid to Write Enable High	75		100		ns
t_{AVEH}	Address Valid to Chip Enable High	75		100		ns
t_{WHQX} (1,2)	Write Enable High to Output Transition	0		0		ns

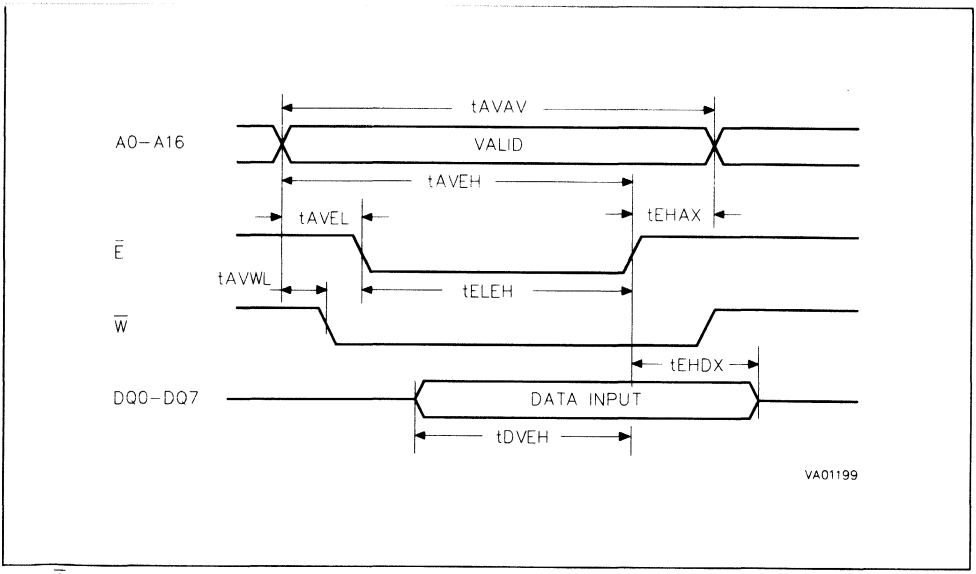
Notes: 1. C_L= 5pF (see Figure 4).
2. If E goes low simultaneously with $\overline{W}$ going low after $\overline{W}$ going low, the outputs remain in the high-impedance state.

Figure 8. Write Enable Controlled, Write AC Waveforms



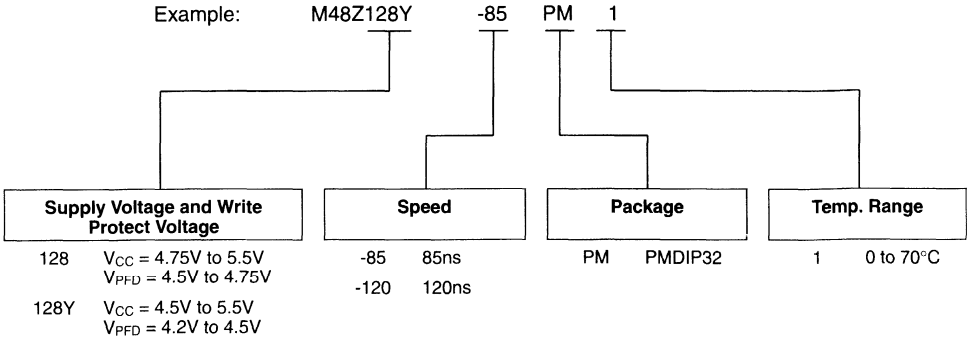
Note: $\overline{G}$ = High.

Figure 9. Chip Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = High.

ORDERING INFORMATION SCHEME



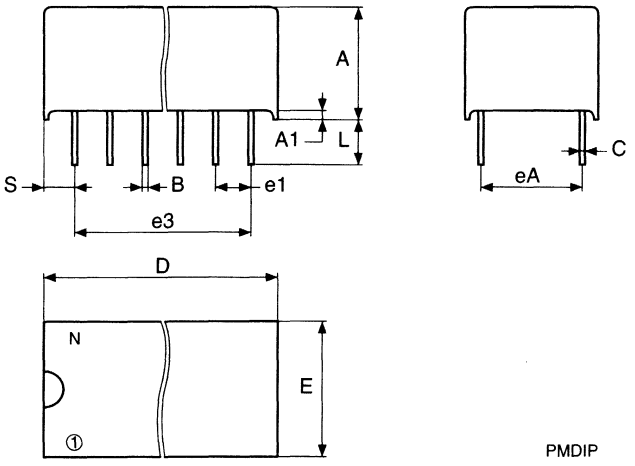
For a list of available options (Package and Speed) refer to the current Memory Shortform catalogue.

For further information or any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PMDIP32 - 32 pin Plastic DIP Module

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		9.27	9.52		0.365	0.375
A1		0.38	–		0.015	–
B		0.43	0.59		0.017	0.023
C		0.20	0.33		0.008	0.013
D		42.42	43.18		1.670	1.700
E		18.03	18.80		0.710	0.740
e1		2.29	2.79		0.090	0.110
e3		34.29	41.91		1.350	1.650
eA		14.99	16.00		0.590	0.630
L		3.05	3.81		0.120	0.150
S		1.91	2.79		0.075	0.110
N	32			32		

PMDIP32

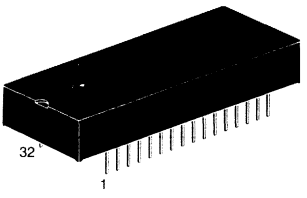


PMDIP

Drawing is not to scale

CMOS 512K x 8 ZEROPOWER SRAM

- INTEGRATED LOW POWER SRAMs, POWER-FAIL CONTROL CIRCUIT and BATTERIES
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 5 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 512K x 8 SRAMs
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z512: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48Z512Y: 4.2V ≤ V_{PFD} ≤ 4.50V
- BATTERIES INTERNALLY ISOLATED UNTIL POWER IS APPLIED



PMLDIP32 (PL)
Module

DESCRIPTION

The M48Z512/512Y 512K x 8 ZEROPOWER® RAM is a non-volatile 4,194,304 bit Static RAM organized as 524,288 words by 8 bits. The device combines two internal lithium batteries and full CMOS SRAMs in a plastic 32 pin DIP long Module.

Table 1. Signal Names

A0 - A18	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

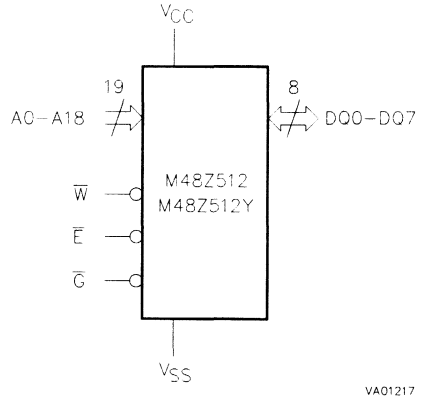


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 70	°C
T_{BIAS}	Temperature Under Bias	–10 to 70	°C
T_{SLD}	Lead Soldering Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

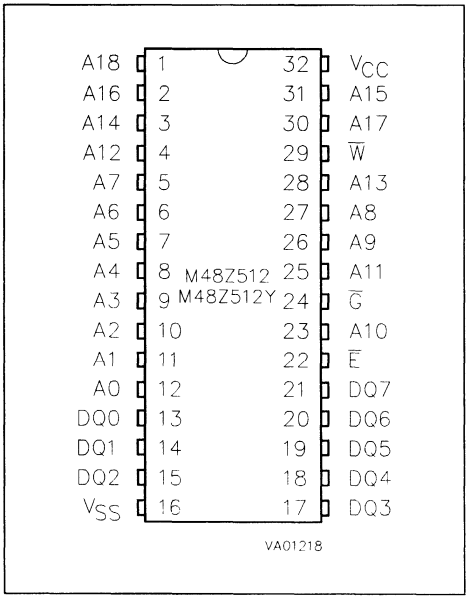
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

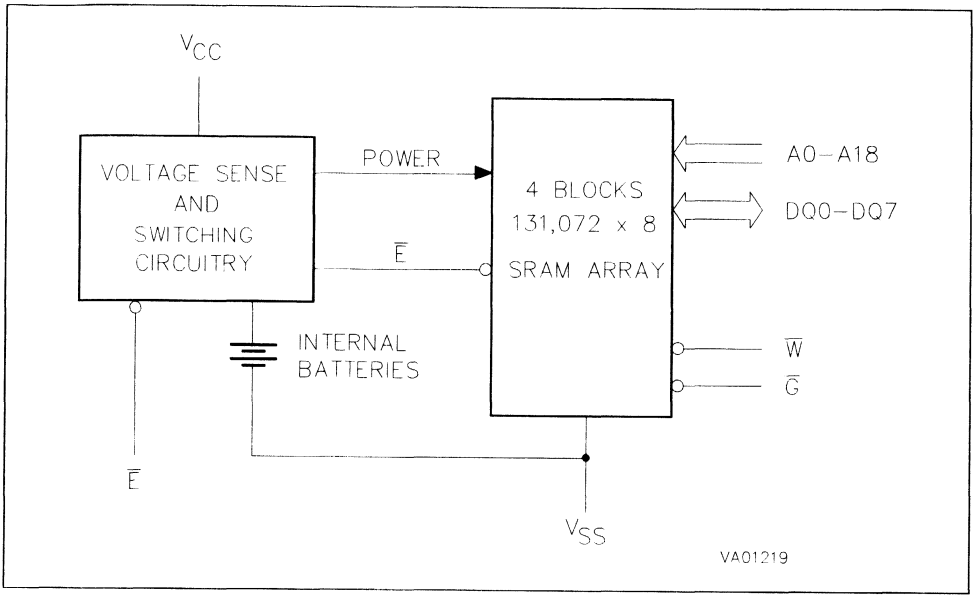
The ZEROPOWER RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z512/512Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the batteries which sustain data until valid power returns.

READ MODE

The M48Z512/512Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 4,194,304 locations in the static storage array. Thus, the unique address specified by the 19 Address Inputs defines which

Figure 3. Block Diagram



one of the 524,288 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48Z512/512Y is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

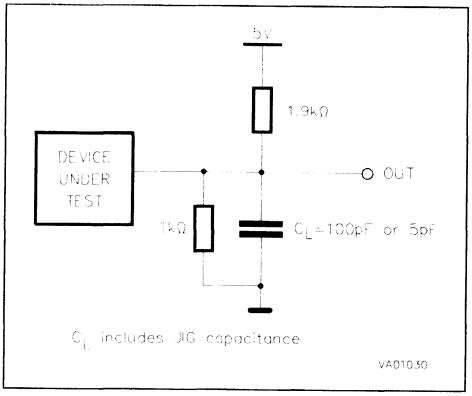


Table 4. Capacitance [1, 2] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		40	pF
C_{IO} [3]	Input / Output Capacitance	V_{OUT} = 0V		40	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±4	µA
I_{LO} [1]	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±4	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, Outputs open		115	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		17	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ ≥ V_{CC} – 0.2V		5	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs deselected.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z512)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z512Y)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3		V
t_{DR} [2]	Data Retention Time	5			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_{WP}	Write Protect Time from V_{CC} = V_{PFD}	40	150	µs
t_R	V_{SO} to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{ER}	$\overline{E}$ Recovery Time	40	120	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

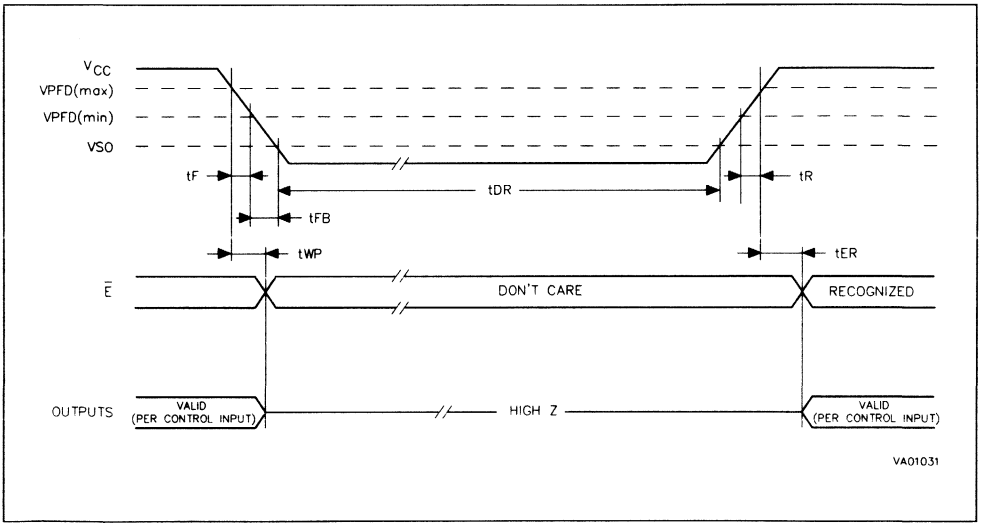
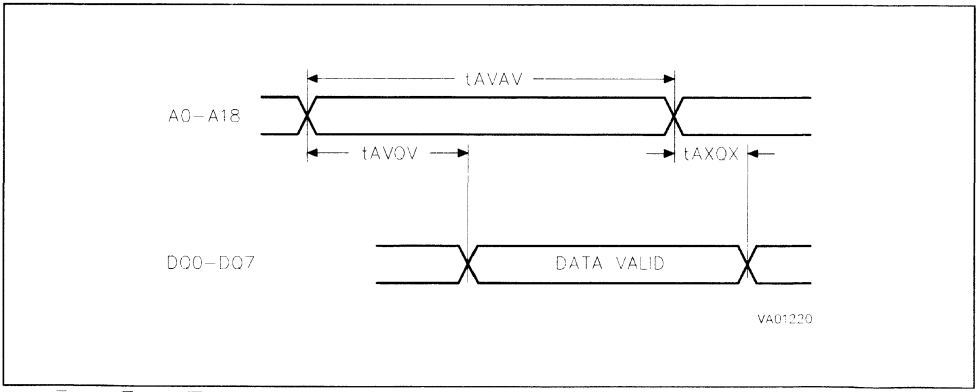


Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z512 / 512Y				Unit
		-85		-120		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	85		120		ns
t_{AVQV} (1)	Address Valid to Output Valid		85		120	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		85		120	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		45		60	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		35		45	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25		35	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		10		ns

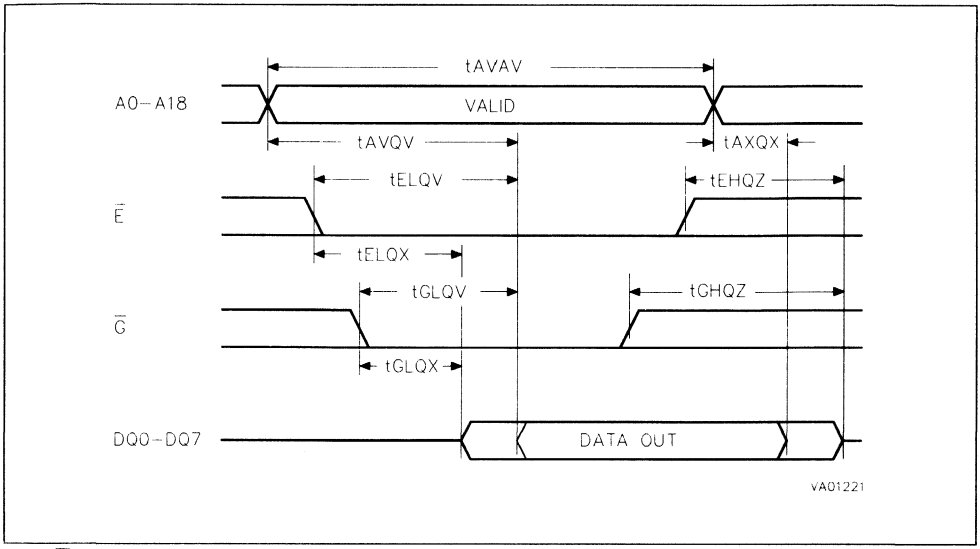
Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4)

Figure 6. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{W}$ = High.

Figure 7. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: $\overline{W}$ = High.

WRITE MODE (cont'd)

The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} or t_{EHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48Z512/512Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data.

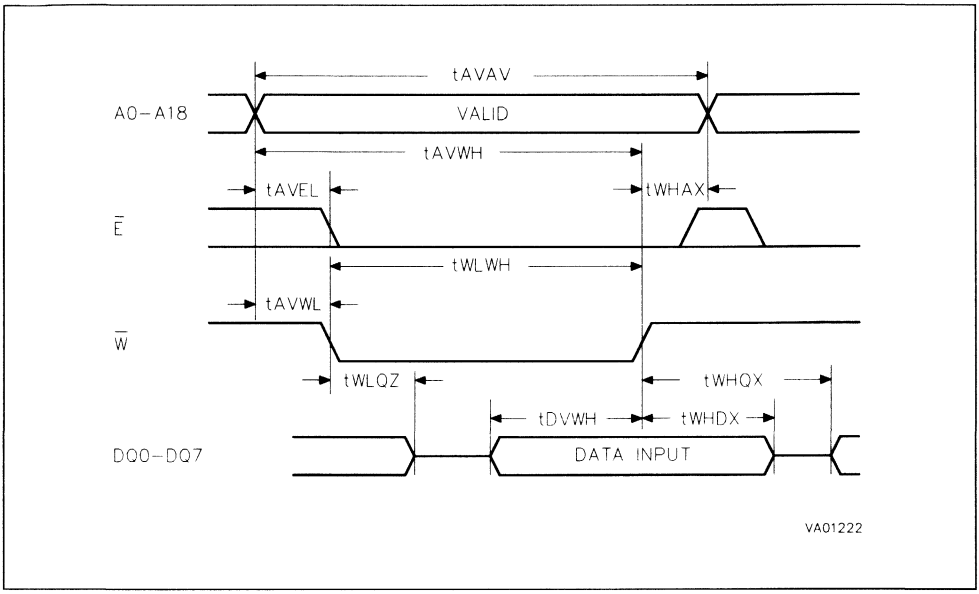
The internal coin cells will maintain data in the M48Z512/512Y after the initial application of V_{CC} for an accumulated period of at least 5 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the batteries are disconnected, and the power supply is switched to external Vcc. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z512 / 512Y				Unit
		-85		-120		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	85		120		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{WLWH}	Write Enable Pulse Width	65		85		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	75		100		ns
t_{WHAX}	Write Enable High to Address Transition	5		5		ns
t_{EHAX}	Chip Enable High to Address Transition	15		15		ns
t_{DVWH}	Input Valid to Write Enable High	35		45		ns
t_{DVEH}	Input Valid to Chip Enable High	35		45		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	10		10		ns
t_{WLQZ} (1,2)	Write Enable Low to Output Hi-Z		30		40	ns
t_{AVWH}	Address Valid to Write Enable High	75		100		ns
t_{AVEH}	Address Valid to Chip Enable High	75		100		ns
t_{WHQX} (1,2)	Write Enable High to Output Transition	0		0		ns

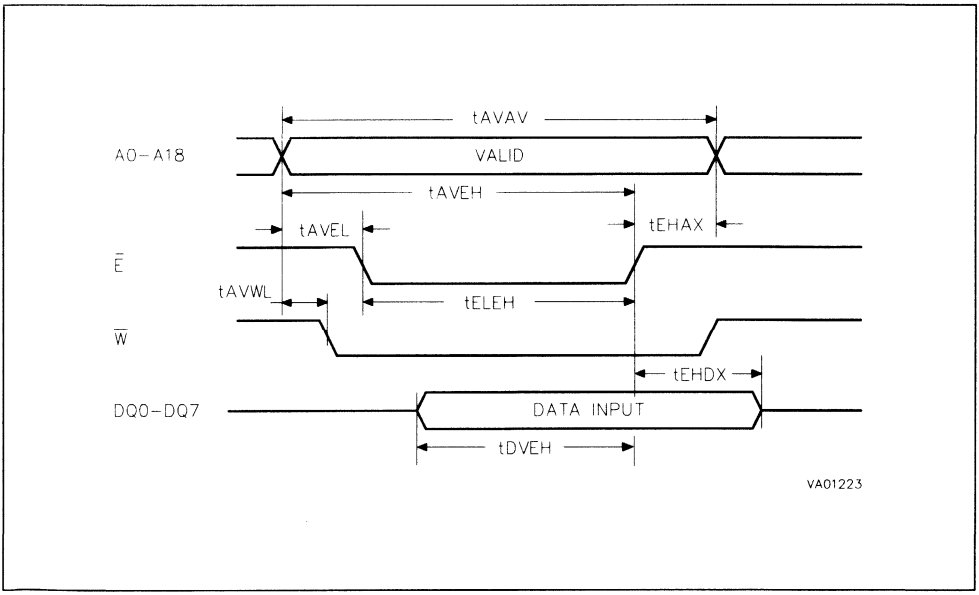
Notes: 1. C_L = 5pF (see Figure 4).
2. If E goes low simultaneously with $\overline{W}$ going low after $\overline{W}$ going low, the outputs remain in the high-impedance state.

Figure 8. Write Enable Controlled, Write AC Waveforms



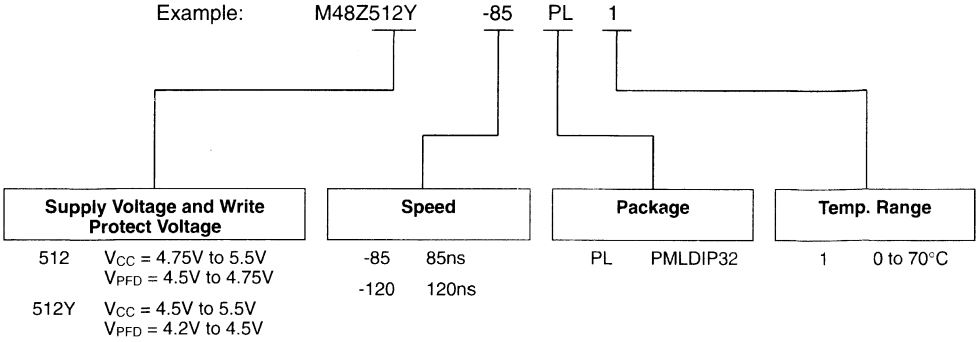
Note: G = High.

Figure 9. Chip Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = High.

ORDERING INFORMATION SCHEME



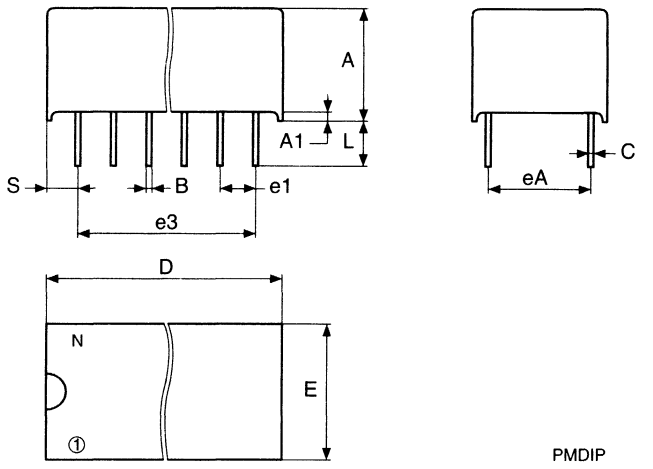
For a list of available options (Package and Speed) refer to the current Memory Shortform catalogue.

For further information or any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PMLDIP32 - 32 pin Plastic DIP Long Module

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		9.27	9.52		0.365	0.375
A1		0.38	–		0.015	–
B		0.43	0.59		0.017	0.023
C		0.20	0.33		0.008	0.013
D		52.58	53.34		2.070	2.100
E		18.03	18.80		0.710	0.740
e1		2.29	2.79		0.090	0.110
e3		34.29	41.91		1.350	1.650
eA		14.99	16.00		0.590	0.630
L		3.05	3.81		0.120	0.150
S		6.99	7.87		0.275	0.310
N	32			32		

PMLDIP32



PMDIP

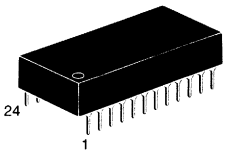
Drawing is not to scale

TIMEKEEPER RAM

M48T02
M48T12

CMOS 2K x 8 TIMEKEEPER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK and POWER-FAIL CONTROL CIRCUIT
- BYTEWIDE RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES and SECONDS
- CLOCK ACCURACY of ± 1 MINUTE a MONTH, @ 25°C
- SOFTWARE CONTROLLED CLOCK CALIBRATION for HIGH ACCURACY APPLICATIONS
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48T02: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48T12: 4.2V ≤ V_{PFD} ≤ 4.5V
- SELF CONTAINED BATTERY and CRYSTAL in the CAPHAT DIP PACKAGE
- 10 YEARS of DATA RETENTION and CLOCK OPERATION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 2K x 8 SRAMs



PCDIP24 (PC)
Battery CAPHAT

DESCRIPTION

The M48T02,12 TIMEKEEPER™ RAM is a 2K x 8 non-volatile static RAM and real time clock which is pin and functional compatible with the MK48T02,12.

Table 1. Signal Names

A0-A10	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

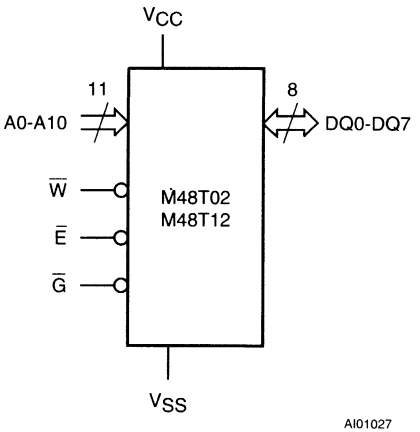


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

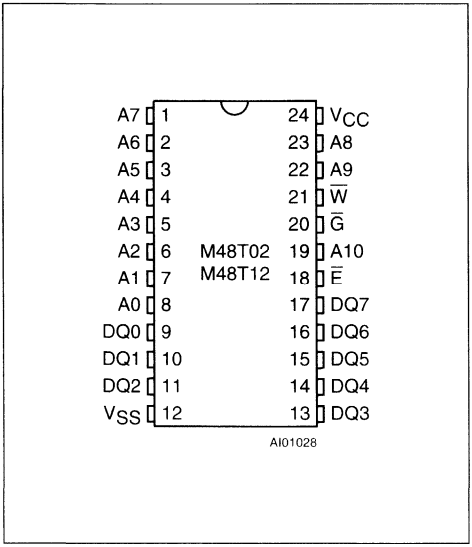
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

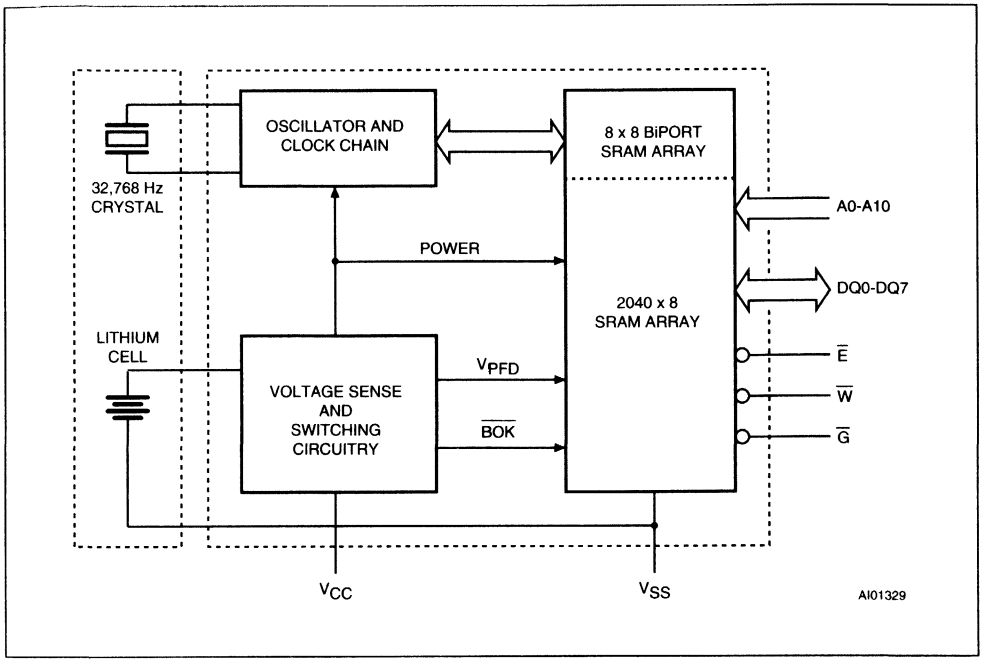
A special 24 pin 600mil DIP CAPHAT™ package houses the M48T02,12 silicon with a quartz crystal and a long life lithium button cell to form a highly integrated battery backed-up memory and real time clock solution.

The M48T02,12 button cell has sufficient capacity and storage life to maintain data and clock functionality for an accumulated time period of at least 10 years in the absence of power over the operating temperature range.

The M48T02,12 is a non-volatile pin and function equivalent to any JEDEC standard 2K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

As Figure 3 shows, the static memory array and the quartz controlled clock oscillator of the M48T02,12 are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE™

Figure 3. Block Diagram



clock information in the bytes with addresses 7F8h-7FFh. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. Byte 7F8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells. The M48T02,12 includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T02,12 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0.6V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

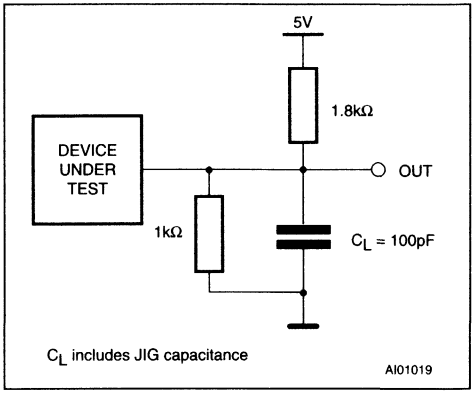


Table 4. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [2]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance calculated from the equation C = IΔt/ΔV with ΔV = 3V and power supply at 5V.
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} [1]	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		80	mA
I_{CC1} [2]	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		3	mA
I_{CC2} [2]	Supply Current (Standby) CMOS	$\overline{E}$ = V_{CC} – 0.2V		3	mA
V_{IL} [3]	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Notes: 1. Outputs Deselected.
2. Measured with Control Bits set as follows: R = '1'; W, ST, KS, FT = '0'.
3. Negative spikes of –1V allowed for up to 10ns once per Cycle.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48T02)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48T12)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} [2]	Expected Data Retention Time	10			YEARS

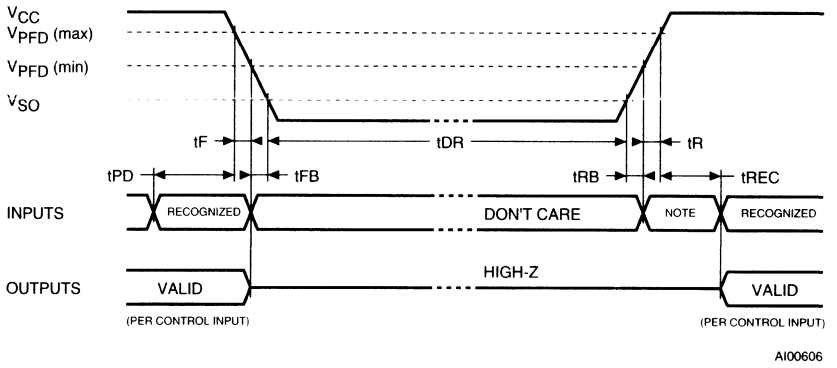
Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 50 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PFD}(min). Some systems may performs inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48T02 / 12						Unit
		-120		-150		-200		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	120		150		200		ns
t_{AVQV}	Address Valid to Output Valid		120		150		200	ns
t_{ELQV}	Chip Enable Low to Output Valid		120		150		200	ns
t_{GLQV}	Output Enable Low to Output Valid		75		75		80	ns
t_{ELQX}	Chip Enable Low to Output Transition	10		10		10		ns
t_{GLQX}	Output Enable Low to Output Transition	5		5		5		ns
t_{EHQZ}	Chip Enable High to Output Hi-Z		30		35		40	ns
t_{GHQZ}	Output Enable High to Output Hi-Z		30		35		40	ns
t_{AXQX}	Address Transition to Output Transition	5		5		5		ns

Figure 6. Read Mode AC Waveforms

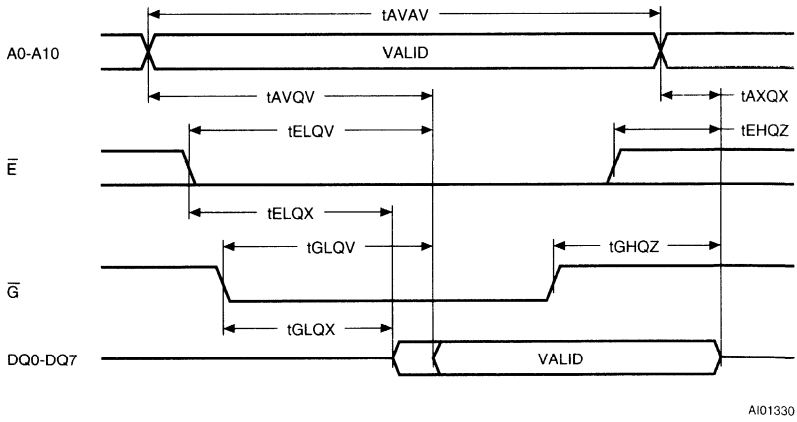


Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48T02 / 12						Unit
		-120		-150		-200		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	120		150		200		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{WLWH}	Write Enable Pulse Width	75		90		120		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	75		90		120		ns
t_{WHAX}	Write Enable High to Address Transition	10		10		10		ns
t_{EHAX}	Chip Enable High to Address Transition	10		10		10		ns
t_{DVWH}	Input Valid to Write Enable High	35		40		60		ns
t_{DVEH}	Input Valid to Chip Enable High	35		40		60		ns
t_{WHDX}	Write Enable High to Input Transition	5		5		5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		5		5		ns
t_{WLQZ}	Write Enable Low to Output Hi-Z		40		50		60	ns
t_{AVWH}	Address Valid to Write Enable High	90		120		140		ns
t_{AVEH}	Address Valid to Chip Enable High	90		120		140		ns
t_{WHQX}	Write Enable High to Output Transition	10		10		10		ns

READ MODE

The M48T02,12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs defines which one of the 2,048 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48T02,12 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 7. Write Enable Controlled, Write AC Waveforms

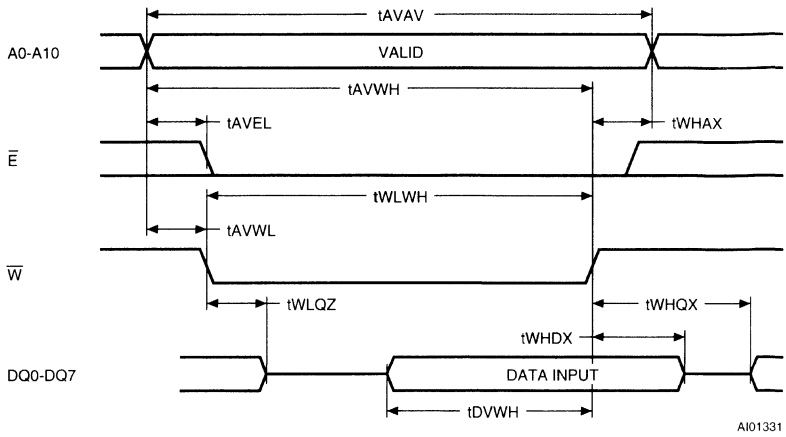
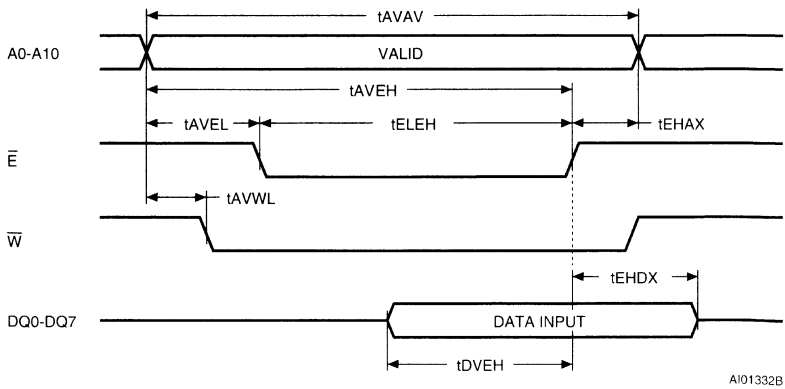


Figure 8. Chip Enable Controlled, Write AC Waveforms



DATA RETENTION MODE

With valid V_{CC} applied, the M48T02,12 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T02,12 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises, the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 9 illustrates how a $\overline{BOK}$ check routine could be structured.

CLOCK OPERATIONS

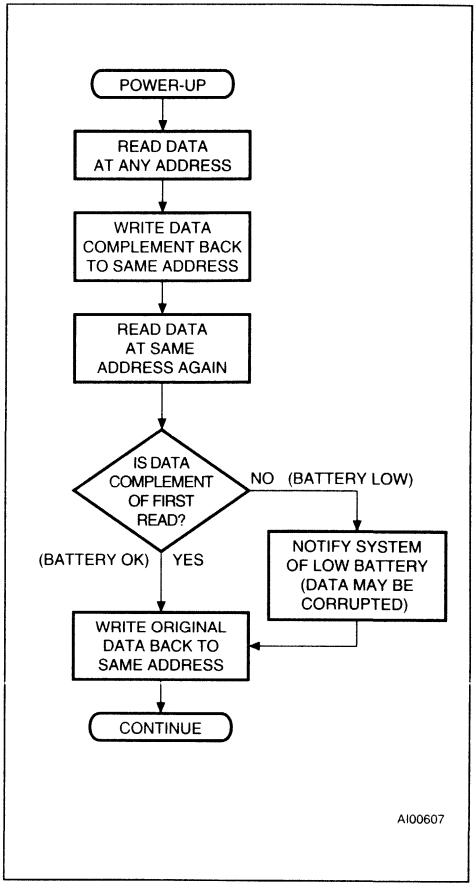
Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, the seventh bit in the control register. As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0'.

Figure 9. Checking the $\overline{BOK}$ Flag Status



Setting the Clock

The eighth bit of the control register is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 10). Resetting the WRITE bit to a '0' then transfers the values of all time registers (7F9h-7FFh) to the actual TIMEKEEPER counters and allows normal operation to resume. The FT bit and the bits marked as '0' in Table 10 must be written to '0' to allow for normal TIMEKEEPER and RAM operation.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T02,12 is shipped from SGS-THOMSON with the STOP bit set to a '1'. When reset to a '0', the M48T02,12 oscillator starts within 1 second.

Calibrating the Clock

The M48T02,12 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. A typical M48T02,12 is accurate within ±1 minute per month at 25°C without calibration. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M48T02,12 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 10. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

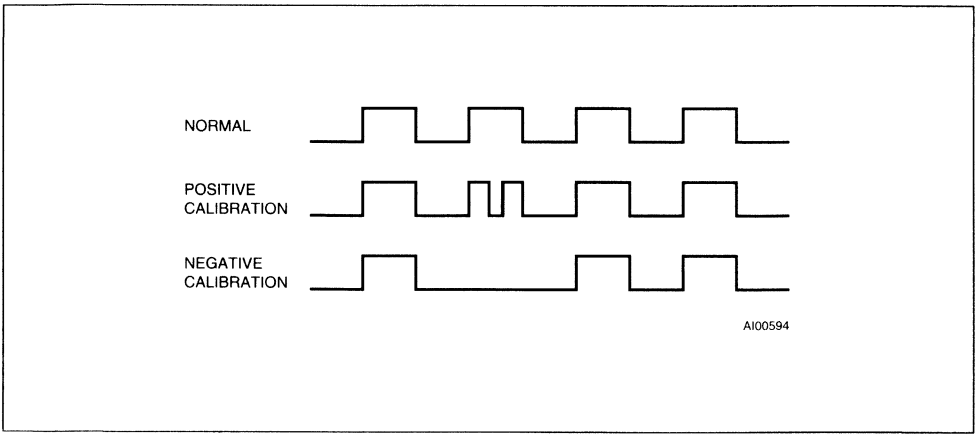
Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or - 2.75 minutes per month.

Table 10. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
7FFh	10 Years				Year				Year	00-99
7FEh	0	0	0	10 M.	Month				Month	01-12
7FDh	0	0	10 Date		Date				Date	01-31
7FCh	0	FT	0	0	0	Day			Day	01-07
7FBh	KS	0	10 Hours		Hours				Hour	00-23
7FAh	0	10 Minutes			Minutes				Minutes	00-59
7F9h	ST	10 Seconds			Seconds				Seconds	00-59
7F8h	W	R	S	Calibration					Control	

Keys: **S** = SIGN Bit
FT = FREQUENCY TEST Bit (Set to '0' for normal clock operation)
KS = KICK START Bit
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to '0'

Figure 10. Clock Calibration

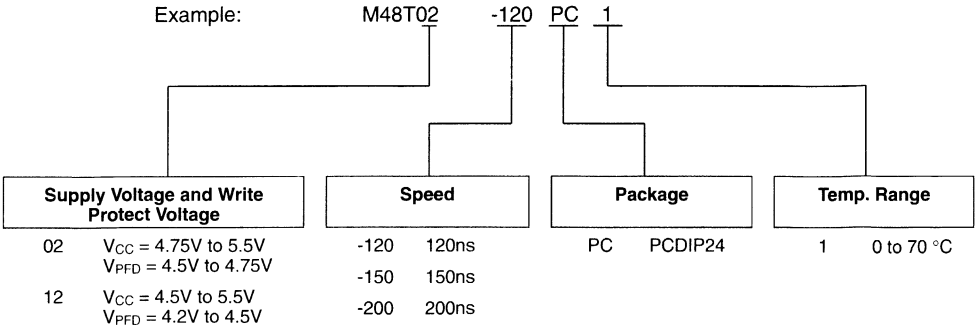


Two methods are available for ascertaining how much calibration a given M48T02,12 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day Register, is set to a '1', and the oscillator is running at 32,768 Hz, the LSB (DQ0) of the Seconds Register will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency. The device must be selected and addresses must stable at Address 7F9h when reading the 512 Hz on DQ0.

The FT bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds Register is monitored by holding the M48T02,12 in an extended read of the Seconds Register, without having the Read bit set. The FT bit MUST be reset to '0' for normal clock operations to resume.

ORDERING INFORMATION SCHEME



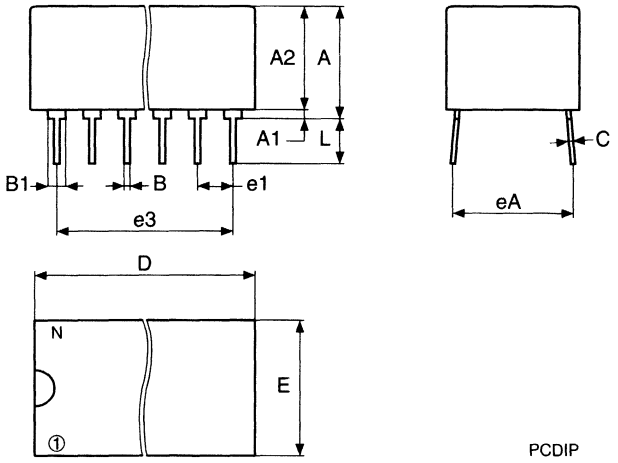
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP24 - 24 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.36	8.89		0.329	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		34.29	34.80		1.350	1.370
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		25.15	30.73		0.990	1.210
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	24			24		

PCDIP24

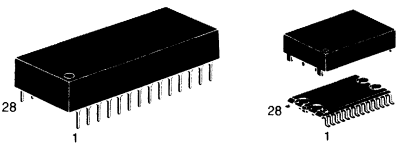


PCDIP

Drawing is not to scale

CMOS 8K x 8 TIMEKEEPER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK and POWER-FAIL CONTROL CIRCUIT
- BYTEWIDE RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES and SECONDS
- CLOCK ACCURACY of ± 1 MINUTE a MONTH, @ 25°C
- SOFTWARE CONTROLLED CLOCK CALIBRATION for HIGH ACCURACY APPLICATIONS
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48T08: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48T18: 4.2V ≤ V_{PFD} ≤ 4.5V
- SELF CONTAINED BATTERY and CRYSTAL in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY and CRYSTAL
- SNAPHAT HOUSING (BATTERY and CRYSTAL) REPLACEABLE
- 10 YEARS of DATA RETENTION and CLOCK OPERATION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 8K x 8 SRAMs



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{INT}$	Power Fail Interrupt
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

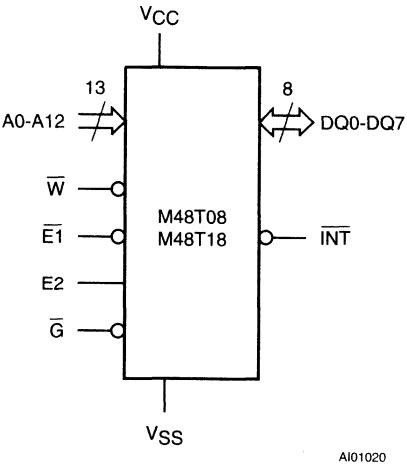


Figure 2A. DIP Pin Connections

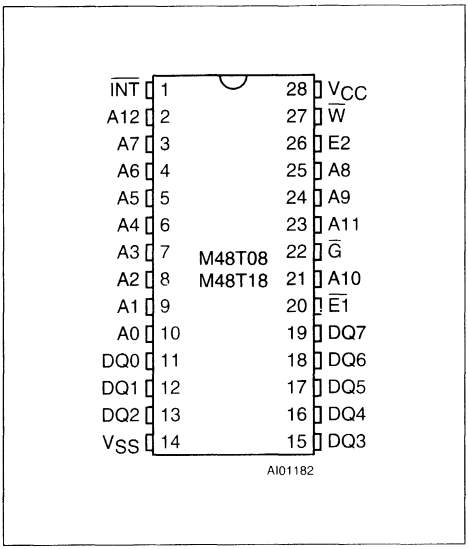


Figure 2B. SO Pin Connections

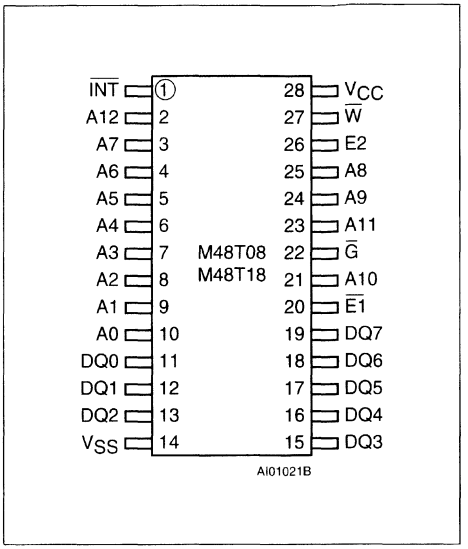


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

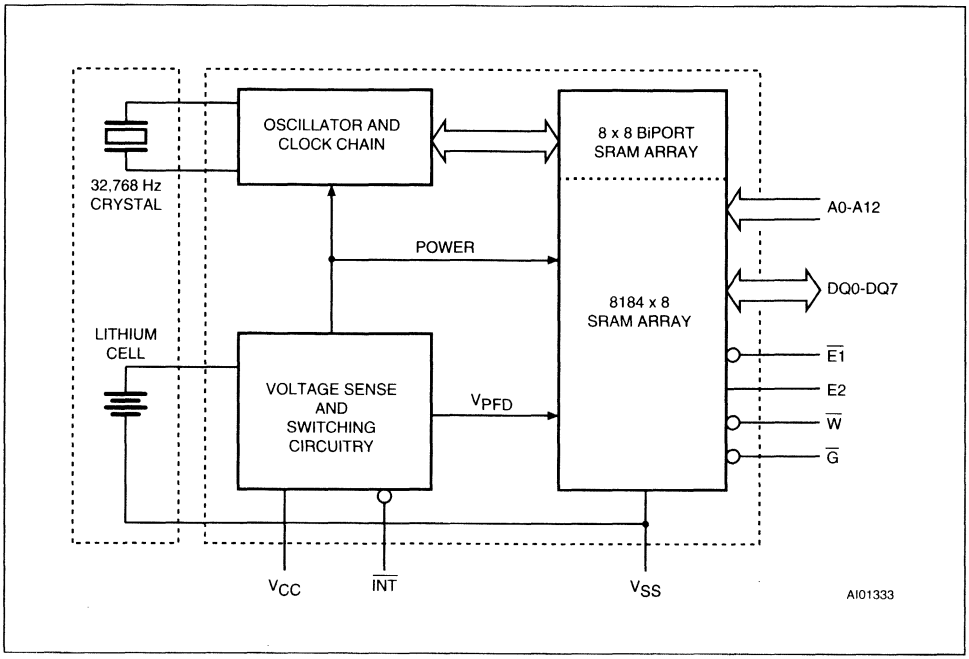
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	X	High Z	Standby
Deselect		X	V_{IL}	X	X	High Z	Standby
Write		V_{IL}	V_{IH}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 3. Block Diagram



DESCRIPTION

The M48T08,18 TIMEKEEPER™ RAM is an 8K x 8 non-volatile static RAM and real time clock which is pin and functional compatible with the MK48T08,18. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory and real time clock solution.

The M48T08,18 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 28 pin 600mil DIP CAPHAT™ houses the M48T08,18 silicon with a quartz crystal and a long life lithium button cell in a single package.

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

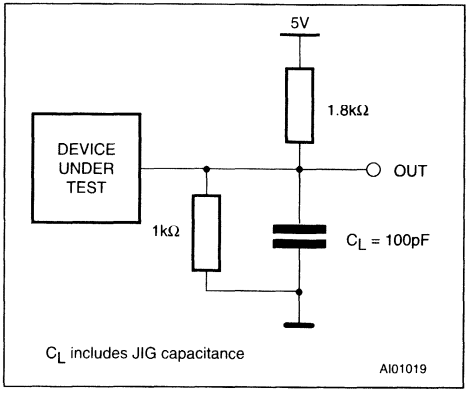


Table 4. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [2]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with ΔV = 3V and power supply at 5V.
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} [1]	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		80	mA
I_{CC1} [2]	Supply Current (Standby) TTL	$\overline{E1}$ = V_{IH}, E2 = V_{IL}		3	mA
I_{CC2} [2]	Supply Current (Standby) CMOS	$\overline{E1}$ = V_{CC} – 0.2V, E2 = V_{SS} + 0.2V		3	mA
V_{IL} [3]	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
	Output Low Voltage ($\overline{INT}$) [4]	I_{OL} = 0.5mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Notes: 1. Outputs Deselected.
2. Measured with Control Bits set as follows: R = '1'; W, ST, FT = '0'.
3. Negative spikes of –1V allowed for up to 10ns once per Cycle.
4. The INT pin is Open Drain.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48T08)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48T18)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} [2]	Expected Data Retention Time	10			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

DESCRIPTION (cont'd)

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T28-BR12SH1".

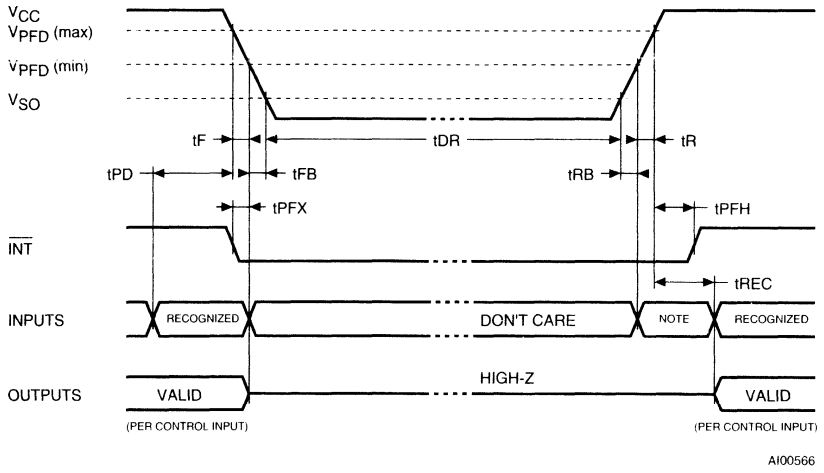
As Figure 3 shows, the static memory array and the quartz controlled clock oscillator of the M48T08,18 are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 1FF8h-1FFFh. The clock locations contain the year, month, date, day, hour, minute, and second in

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E1}$ or $\overline{W}$ at V_{IH} or E2 at V_{IL} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	$\overline{E1}$ or $\overline{W}$ at V_{IH} or E2 at V_{IL} after Power Up	1		ms
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	µs
t_{PFH} (3)	V_{PFD} (max) to $\overline{INT}$ High		120	µs

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.
3. INT may go high anytime after V_{CC} exceeds V_{PFD} (min) and is guaranteed to go high t_{PFH} after V_{CC} exceeds V_{PFD} (max).

Figure 5. Power Down/Up Mode AC Waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep E1 high or E2 low as V_{CC} rises past V_{PFD}(min). Some systems may performs inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

Table 8. Read Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48T08 / 18				Unit
		-100		-150		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	100		150		ns
t_{AVQV}	Address Valid to Output Valid		100		150	ns
t_{E1LQV}	Chip Enable 1 Low to Output Valid		100		150	ns
t_{E2HQV}	Chip Enable 2 High to Output Valid		100		150	ns
t_{GLQV}	Output Enable Low to Output Valid		50		75	ns
t_{E1LQX}	Chip Enable 1 Low to Output Transition	10		10		ns
t_{E2HQX}	Chip Enable 2 High to Output Transition	10		10		ns
t_{GLQX}	Output Enable Low to Output Transition	5		5		ns
t_{E1HQZ}	Chip Enable 1 High to Output Hi-Z		50		75	ns
t_{E2LQZ}	Chip Enable 2 Low to Output Hi-Z		50		75	ns
t_{GHQZ}	Output Enable High to Output Hi-Z		40		60	ns
t_{AXQX}	Address Transition to Output Transition	5		5		ns

Figure 6. Read Mode AC Waveforms

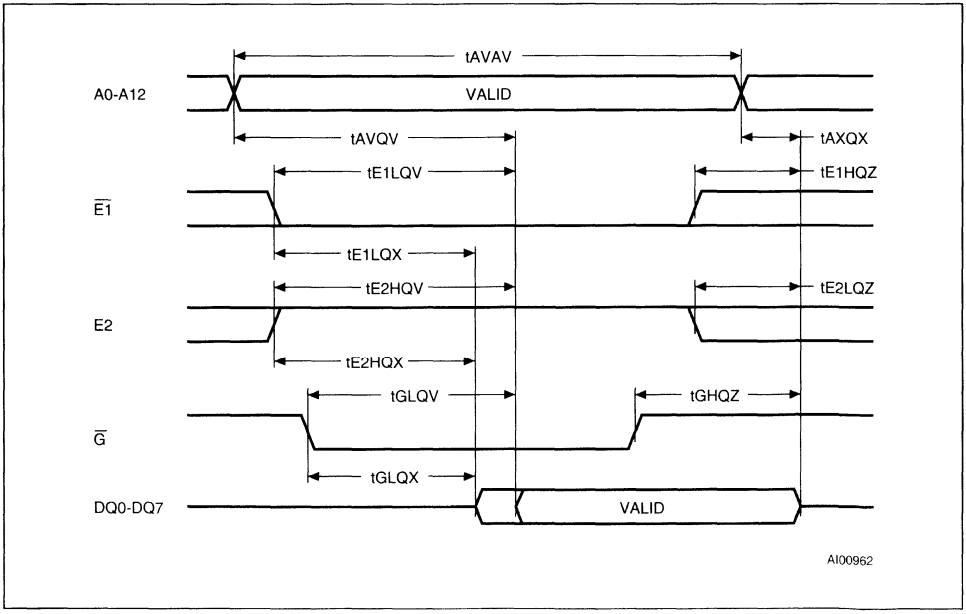


Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48T08 / 18				Unit
		-100		-150		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	100		150		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVE1L}	Address Valid to Chip Enable 1 Low	0		0		ns
t_{AVE2H}	Address Valid to Chip Enable 2 High	0		0		ns
t_{WLWH}	Write Enable Pulse Width	80		100		ns
t_{E1LE1H}	Chip Enable 1 Low to Chip Enable 1 High	80		130		ns
t_{E2HE2L}	Chip Enable 2 High to Chip Enable 2 Low	80		130		ns
t_{WHAX}	Write Enable High to Address Transition	10		10		ns
t_{E1HAX}	Chip Enable 1 High to Address Transition	10		10		ns
t_{E2LAX}	Chip Enable 2 Low to Address Transition	10		10		ns
t_{DVWH}	Input Valid to Write Enable High	50		70		ns
t_{DVE1H}	Input Valid to Chip Enable 1 High	50		70		ns
t_{DVE2L}	Input Valid to Chip Enable 2 Low	50		70		ns
t_{WHDX}	Write Enable High to Input Transition	5		5		ns
t_{E1HDX}	Chip Enable 1 High to Input Transition	5		5		ns
t_{E2LDX}	Chip Enable 2 Low to Input Transition	5		5		ns
t_{WLQZ}	Write Enable Low to Output Hi-Z		50		70	ns
t_{AVWH}	Address Valid to Write Enable High	80		130		ns
t_{AVE1H}	Address Valid to Chip Enable 1 High	80		130		ns
t_{AVE2L}	Address Valid to Chip Enable 2 Low	80		130		ns
t_{WHQX}	Write Enable High to Output Transition	10		10		ns

Figure 7. Write Enable Controlled, Write AC Waveforms

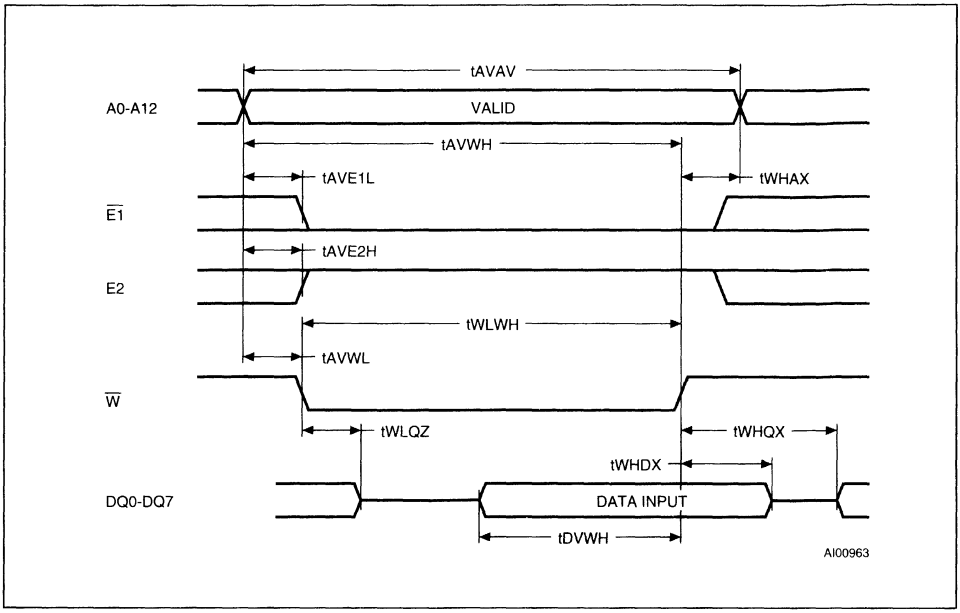
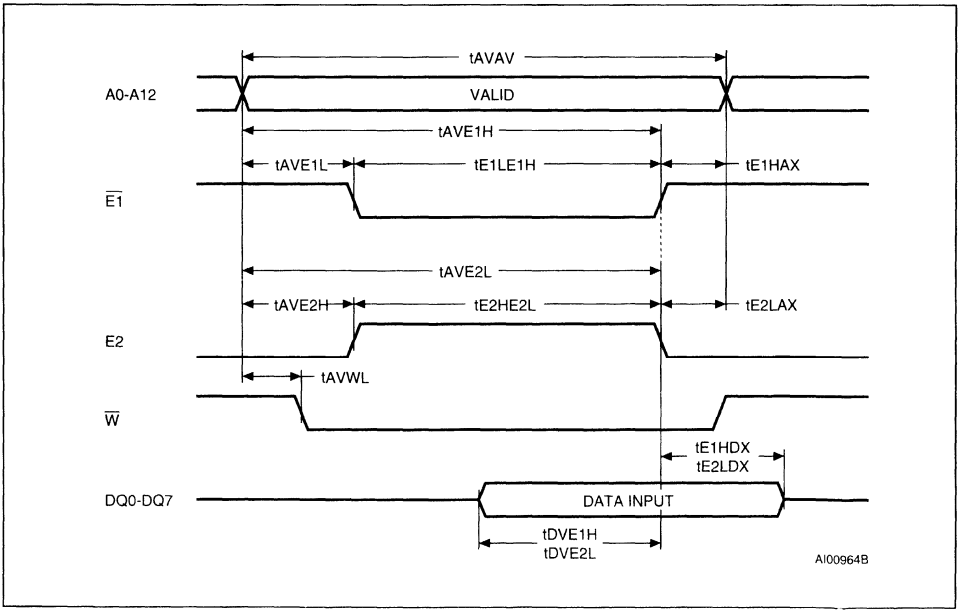


Figure 8. Chip Enable Controlled, Write AC Waveforms



DESCRIPTION (cont'd)

24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. Byte 1FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells. The M48T08,18 includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T08,18 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

READ MODE

The M48T08,18 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E1}$ (Chip Enable 1) is low, and E2 (Chip Enable 2) is high. The device architecture allows ripple- through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E1}$, E2, and $\overline{G}$ access times are also satisfied. If the $\overline{E1}$, E2 and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Times (t_{E1LQV} or t_{E2HQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E1}$, E2 and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E1}$, E2 and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48T08,18 is in the Write Mode whenever $\overline{W}$, $\overline{E1}$, and E2 are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E1}$, or the rising edge of E2. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E1}$, or the falling edge of E2. The addresses must be held valid throughout the cycle. $\overline{E1}$ or $\overline{W}$ must return high or E2 low for minimum of t_{E1HAX} or t_{E2LAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E1}$ and $\overline{G}$ and a high on E2, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48T08,18 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T08,18 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T08,18 for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD}(min). $\overline{E1}$ should be kept high or E2 low as V_{CC} rises past V_{PFD}(min) to prevent inadvertent write cycles prior to processor stabilization. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max).

POWER FAIL INTERRUPT PIN

The M48T08,18 continuously monitors V_{CC}. When V_{CC} falls to the power-fail detect trip point, an interrupt is immediately generated. An internal clock provides a delay of between 10µs and 40µs before automatically deselecting the M48T08,18. The $\overline{INT}$ pin is an open drain output and requires an external pull up resistor, even if the interrupt output function is not being used.

SYSTEM BATTERY LIFE

The useful life of the battery in the M48T08,18 is expected to ultimately come to an end for one of two reasons: either because it has been discharged while providing current to the RAM and clock in the battery back-up mode, or because the effects of aging render the cell useless before it can actually be completely discharged. The two effects are virtually unrelated allowing discharge, or Capacity Consumption, and the effects of aging, or Storage Life, to be treated as two independent but simultaneous mechanisms. The earlier occurring failure mechanism defines the battery system life of the M48T08,18.

Cell Storage Life

Storage life is primarily a function of temperature. Figure 9 illustrates the approximate storage life of the M48T08,18 battery over temperature. The results in Figure 9 are derived from temperature accelerated life test studies performed at SGS-THOMSON. For the purpose of the testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4V closed circuit voltage across a 250 kΩ load resistor. The two lines, $t_{1\%}$ and $t_{50\%}$, represent different failure rate distributions for the cell's storage life. At 70°C, for example, the $t_{1\%}$ line indicates that an M48T08,18 has a 1% chance of having a battery failure 11 years into its life while the $t_{50\%}$ shows the part has a 50% chance of failure at the 20 year mark. The $t_{1\%}$ line represents the practical onset of wear out and can be considered the worst case Storage Life for the cell. The $t_{50\%}$ can be considered the normal or average life.

Calculating Storage Life

The following formula can be used to predict storage life:

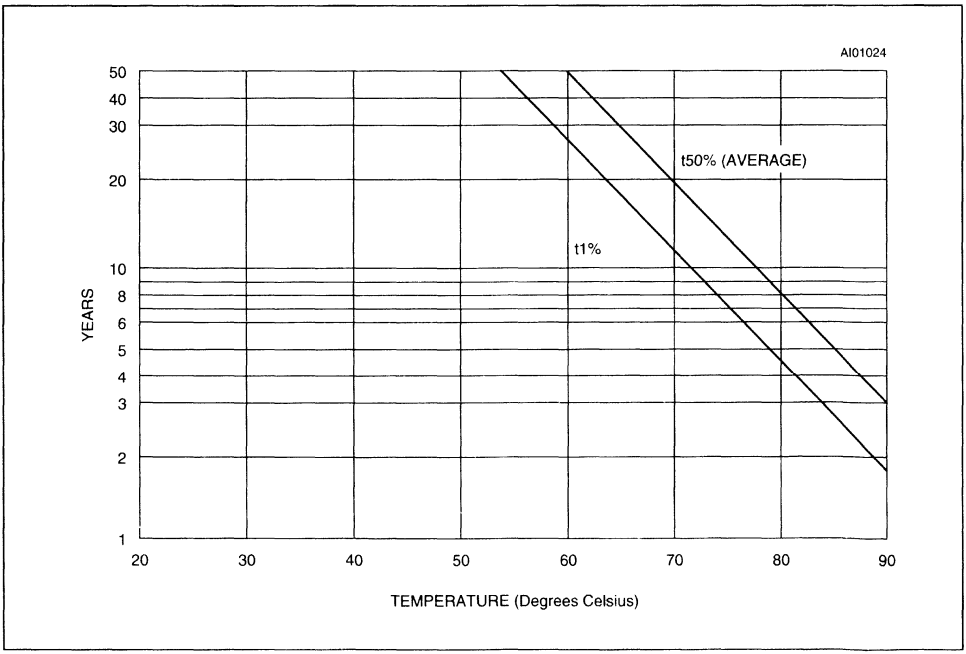
$$\frac{1}{\{[(TA1/TT)/SL1]+[(TA2/TT)/SL2]+...+[(TAN/TT)/SLN]\}}$$

where,

- TA1, TA2, TAN = time at ambient temperature 1, 2, etc.
- TT = total time = TA1+TA2+...+TAN
- SL1, SL2, SLN = storage life at temperature 1, 2, etc.

For example an M48T08,18 is exposed to temperatures of 55°C or less for 8322 hrs/yr, and temperatures greater than 60°C but less than 70°C for the remaining 438 hrs/yr. Reading predicted $t_{1\%}$ values from Figure 9,

Figure 9. Predicted Battery Storage Life versus Temperature



– SL1 = 41 yrs, SL2 = 11.4 yrs

– TT = 8760 hrs/yr

– TA1 = 8322 hrs/yr, TA2 = 438 hrs/yr

Predicted storage life ≥

$$\frac{1}{\{[(8322/8760)/41]+[(431/8760)/11.4]\}}$$

or 36 years.

Cell Capacity Life

The M48T08,18 internal cell has a rated capacity of 50mAh. The device places a nominal RAM and TIMEKEEPER load of less than 520nA at room temperature. At this rate, the capacity consumption life is 50E-3/520E-9 = 96,153 hours or about 11 years. Capacity consumption life can be extended by applying V_{CC} or turning off the clock oscillator prior to system power down.

Calculating Capacity Life

The RAM and TIMEKEEPER load remains relatively constant over the operating temperature range. Thus, worst case cell capacity life is essentially a function of one variable, V_{CC} duty cycle. For example, if the oscillator runs 100% of the time with V_{CC} applied 60% of the time, the capacity consumption life is 10/(1-0.6), or 25 years.

Estimated System Life

Since either storage life or capacity consumption can end the battery's life, the system life is marked by which ever occurs first. In the above example, this would be 25 years.

Reference for System Life

Each M48T08,18 is marked with a nine digit manufacturing date code in the form of H99XXYYZZ. For example, H995B9431 is:

H = fabricated in Carrollton, TX

9 = assembled in Muar, Malaysia,

9 = tested in Muar, Malaysia,

5B = lot designator,

9431 = assembled in the year 1994, work week 31.

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, the seventh bit in the control register. As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0'.

Setting the Clock

The eighth bit of the control register is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 10). Resetting the WRITE bit to a '0' then transfers the values of all time registers (1FF9h-1FFFh) to the actual TIMEKEEPER counters and allows normal operation to resume. The FT bit and the bits marked as '0' in Table 10 must be written to '0' to allow for normal TIMEKEEPER and RAM operation.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T08,18 is shipped from SGS-THOMSON with the STOP bit set to a '1'. When reset to a '0', the M48T08,18 oscillator starts within 1 second.

Calibrating the Clock

The M48T08,18 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. A typical M48T08,18 is accurate within ±1 minute per month at 25°C without calibration. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature. Figure 11 shows the frequency error that can be expected at various temperatures. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M48T08,18 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 10. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary

CLOCK OPERATIONS (cont'd)

form. The sixth bit is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or - 2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48T08,18 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day Register, is set to a '1', and the oscillator is running at 32,768 Hz, the LSB (DQ0) of the Seconds Register will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency. The device must be selected and addresses must stable at Address 1FF9h when reading the 512 Hz on DQ0.

The FT bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds Register is monitored by holding the M48T08,18 in an extended read of the Seconds Register, without having the Read bit set. The FT bit MUST be reset to '0' for normal clock operations to resume.

Table 10. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
1FFFh	10 Years				Year				Year	00-99
1FFEh	0	0	0	10 M.	Month				Month	01-12
1FFDh	0	0	10 Date		Date				Date	01-31
1FFCh	0	FT	0	0	0	Day			Day	01-07
1FFBh	0	0	10 Hours		Hours				Hour	00-23
1FFAh	0	10 Minutes			Minutes				Minutes	00-59
1FF9h	ST	10 Seconds			Seconds				Seconds	00-59
1FF8h	W	R	S	Calibration					Control	

Keys: **S** = SIGN Bit
FT = FREQUENCY TEST Bit (Set to '0' for normal clock operation)
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to '0'

Figure 10. Clock Calibration

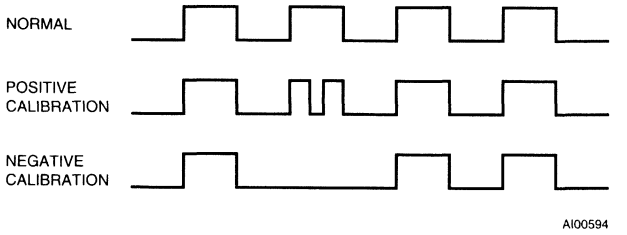
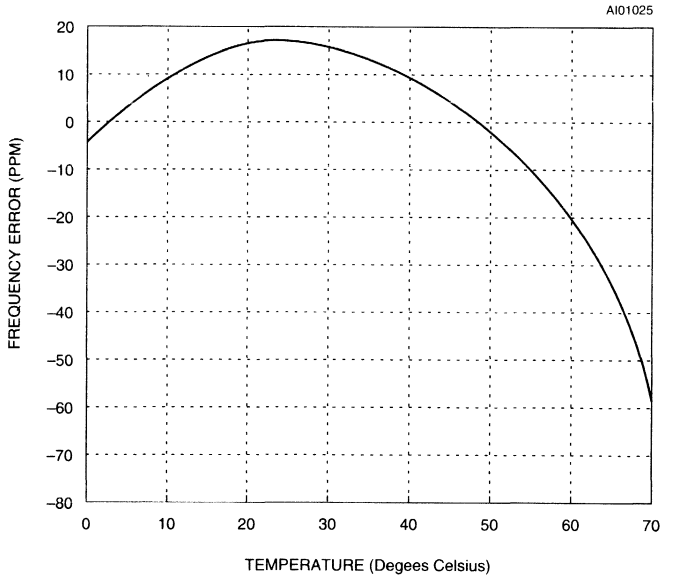
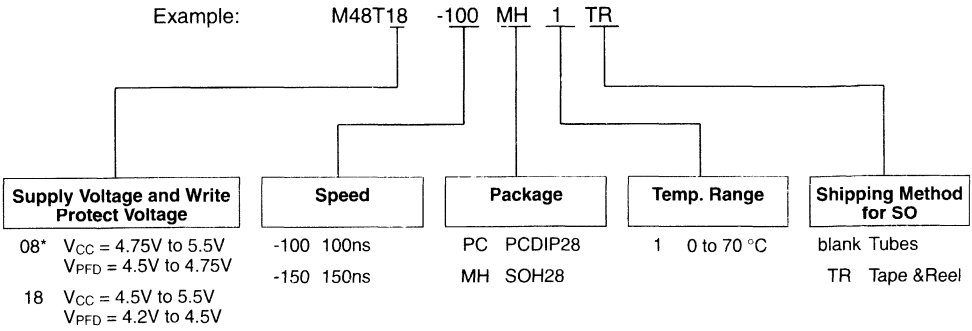


Figure 11. Crystal Frequency Error



ORDERING INFORMATION SCHEME



Note: 08* CAPHAT package only.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the M48T18 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T28-BR12SH1".

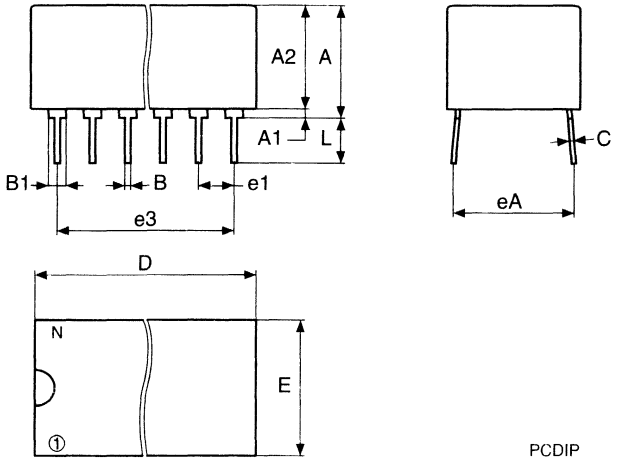
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP28 - 28 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

PCDIP28



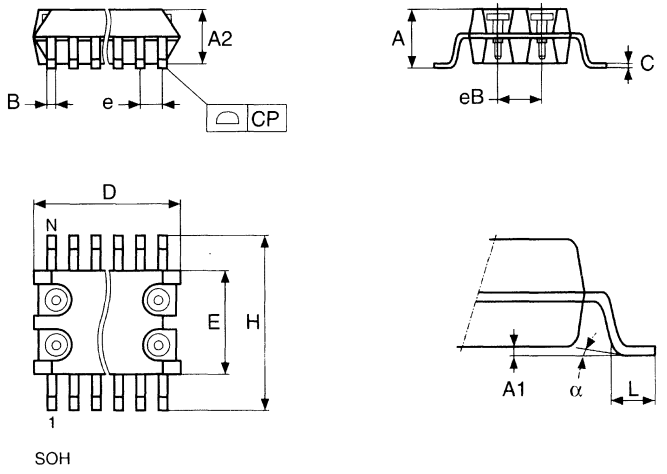
PCDIP

Drawing is not to scale

SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N		28			28	
CP			0.10			0.004

SOH28



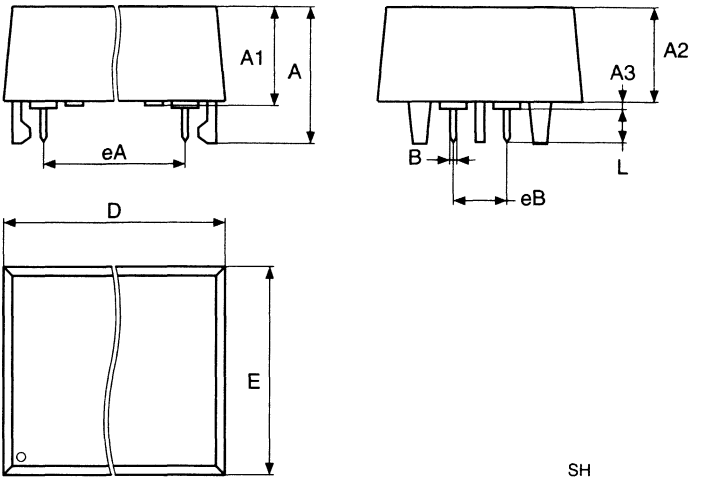
SOH

Drawing is not to scale

SH28 - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

SH28

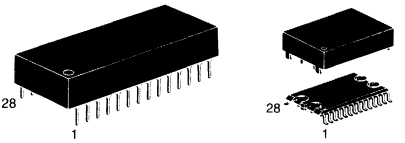


SH

Drawing is not to scale

CMOS 8K x 8 TIMEKEEPER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT and BATTERY
- BYTEWIDE RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES and SECONDS
- FREQUENCY TEST OUTPUT for REAL TIME CLOCK
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48T58: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48T58Y: 4.2V ≤ V_{PFD} ≤ 4.5V
- SELF CONTAINED BATTERY and CRYSTAL in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY and CRYSTAL
- SNAPHAT HOUSING (BATTERY and CRYSTAL) REPLACEABLE
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 8K x 8 SRAMs



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

Figure 1. Logic Diagram

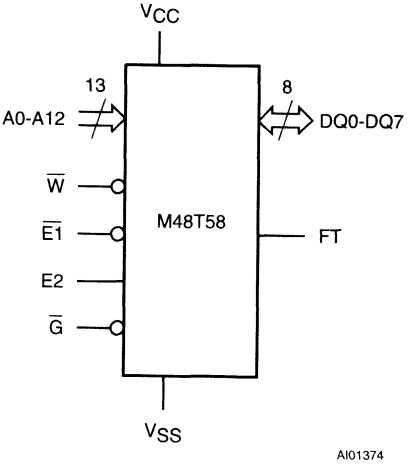


Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
FT	Frequency Test Output (Open Drain)
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

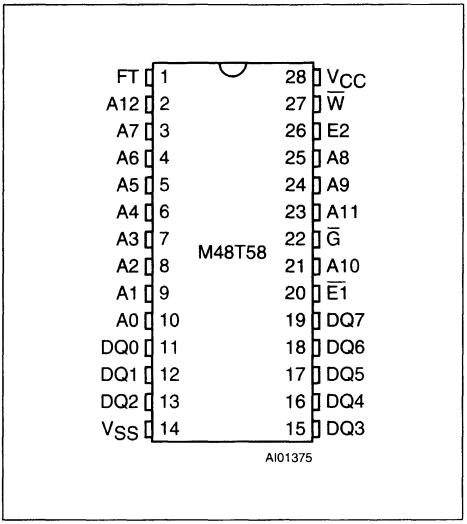


Figure 2B. SO Pin Connections

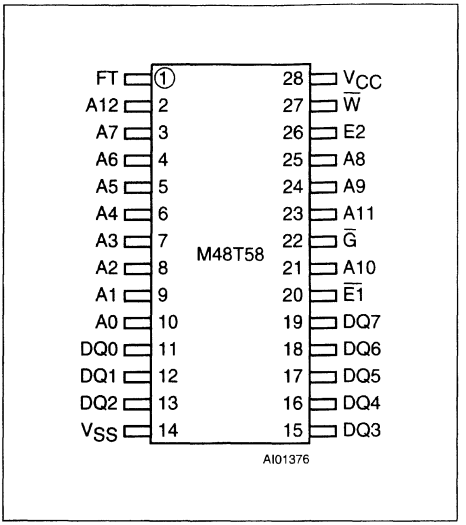


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

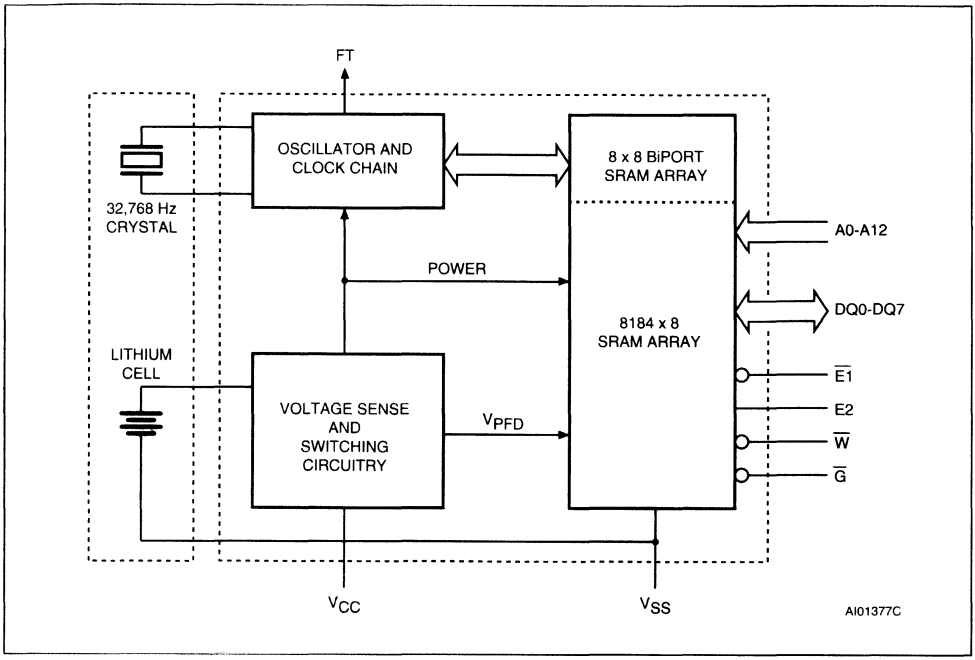
Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes (1)

Mode	V_{CC}	$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	X	High Z	Standby
Deselect		X	V_{IL}	X	X	High Z	Standby
Write		V_{IL}	V_{IH}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min) (2)	X	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	X	High Z	Battery Back-up Mode

Notes: 1. X = V_{IH} or V_{IL}
2. See Table 6 for details.

Figure 3. Block Diagram



DESCRIPTION

The M48T58 TIMEKEEPER™ RAM is an 8K x 8 non-volatile static RAM and real time clock. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory and real time clock solution.

The M48T58 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 28 pin 600mil DIP CAPHAT™ houses the M48T58 silicon with a quartz crystal and a long life lithium button cell in a single package.

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

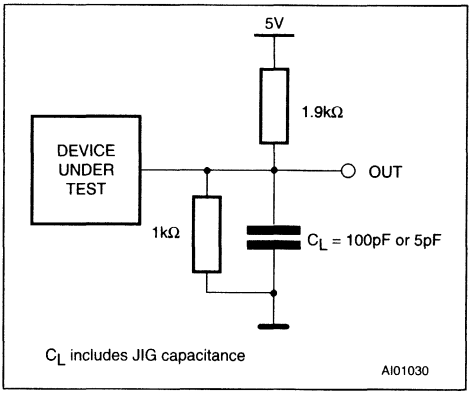


Table 4. Capacitance [1, 2] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [3]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} [1]	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E1}$ = V_{IH}, E2 = V_{IL}		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E1}$ = V_{CC} − 0.2V, E2 = V_{SS} + 0.2V		3	mA
V_{IL} [2]	Input Low Voltage		−0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
	Output Low Voltage (FT) [3]	I_{OL} = 10mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1mA	2.4		V

Notes: 1. Outputs Deselected.
2. Negative spikes of −1V allowed for up to 10ns once per Cycle.
3. The FT pin is Open Drain.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48T58)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48T58Y)	4.2	4.35	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} [2]	Expected Data Retention Time	7			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

DESCRIPTION (cont'd)

to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T28-BR12SH1".

As Figure 3 shows, the static memory array and the quartz controlled clock oscillator of the M48T58 are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E1}$ or $\overline{W}$ at V_{IH} or E2 at V_{IL} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	10		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	V_{PFD}(max) to Inputs Recognized	40	200	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

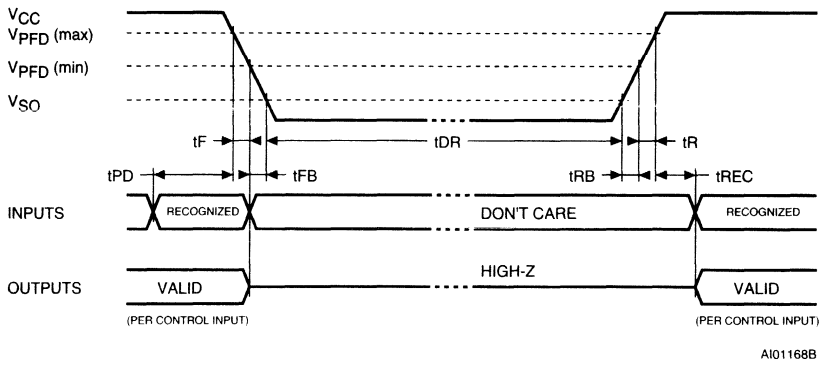
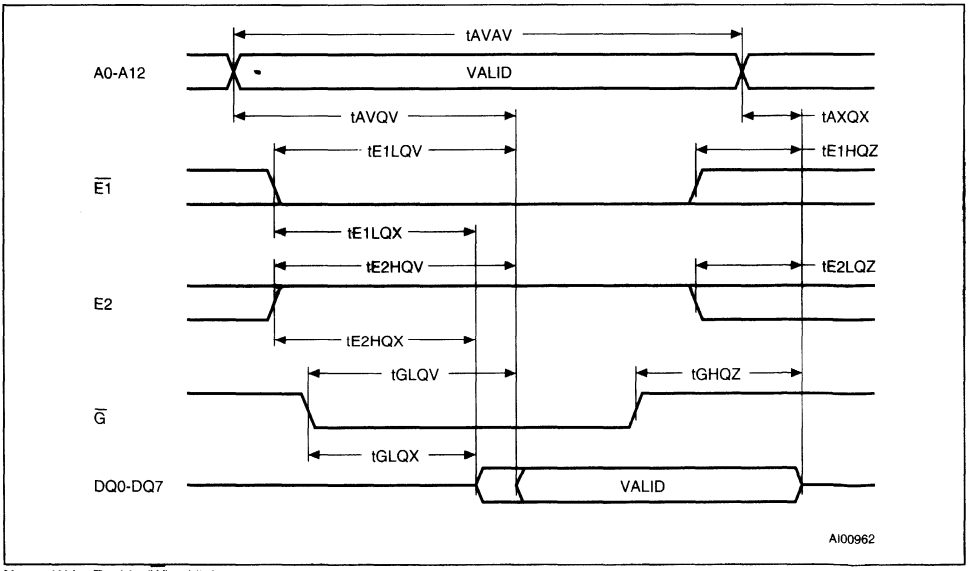


Table 8. Read Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48T58 / 58Y		Unit
		-70		
		Min	Max	
t_{AVAV}	Read Cycle Time	70		ns
t_{AVQV} (1)	Address Valid to Output Valid		70	ns
t_{E1LQV} (1)	Chip Enable 1 Low to Output Valid		70	ns
t_{E2HQV} (1)	Chip Enable 2 High to Output Valid		70	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		35	ns
t_{E1LQX} (2)	Chip Enable 1 Low to Output Transition	5		ns
t_{E2HQX} (2)	Chip Enable 2 High to Output Transition	5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		ns
t_{E1HQZ} (2)	Chip Enable 1 High to Output Hi-Z		25	ns
t_{E2LQZ} (2)	Chip Enable 2 Low to Output Hi-Z		25	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		ns

Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4).

Figure 6. Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High

Table 9. Write Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48T58 / 58Y		Unit
		-70		
		Min	Max	
t_{AVAV}	Write Cycle Time	70		ns
t_{AVWL}	Address Valid to Write Enable Low	0		ns
t_{AVE1L}	Address Valid to Chip Enable 1 Low	0		ns
t_{AVE2H}	Address Valid to Chip Enable 2 High	0		ns
t_{WLWH}	Write Enable Pulse Width	50		ns
t_{E1LE1H}	Chip Enable 1 Low to Chip Enable 1 High	55		ns
t_{E2HE2L}	Chip Enable 2 High to Chip Enable 2 Low	55		ns
t_{WHAX}	Write Enable High to Address Transition	0		ns
t_{E1HAX}	Chip Enable 1 High to Address Transition	0		ns
t_{E2LAX}	Chip Enable 2 Low to Address Transition	0		ns
t_{DVWH}	Input Valid to Write Enable High	30		ns
t_{DVE1H}	Input Valid to Chip Enable 1 High	30		ns
t_{DVE2L}	Input Valid to Chip Enable 2 Low	30		ns
t_{WHDX}	Write Enable High to Input Transition	5		ns
t_{E1HDX}	Chip Enable 1 High to Input Transition	5		ns
t_{E2LDX}	Chip Enable 2 Low to Input Transition	5		ns
t_{WLQZ} (1, 2)	Write Enable Low to Output Hi-Z		25	ns
t_{AVWH}	Address Valid to Write Enable High	60		ns
t_{AVE1H}	Address Valid to Chip Enable 1 High	60		ns
t_{AVE2L}	Address Valid to Chip Enable 2 Low	60		ns
t_{WHQX} (1, 2)	Write Enable High to Output Transition	5		ns

Notes: 1. C_L = 5pF (see Figure 4).
2. If $\overline{E1}$ goes low or E2 high simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

Figure 7. Write Enable Controlled, Write AC Waveforms

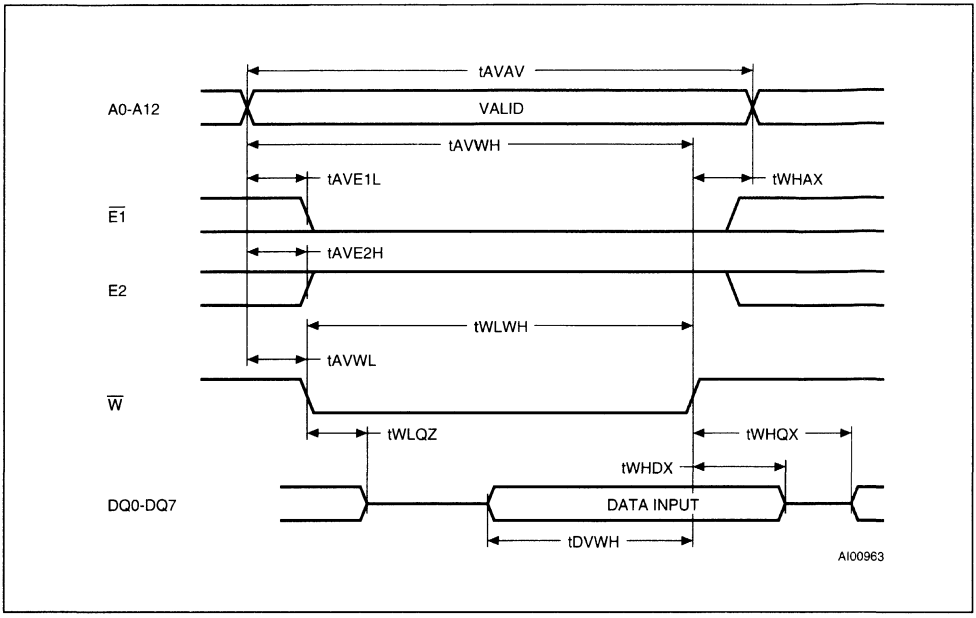
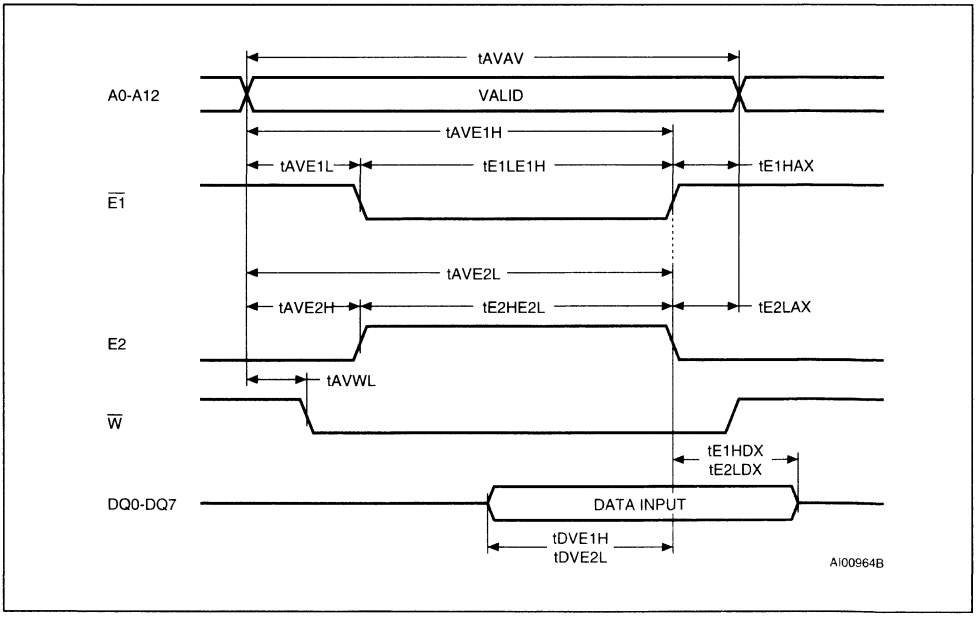


Figure 8. Chip Enable Controlled, Write AC Waveforms



DESCRIPTION (cont'd)

to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 1FF8h-1FFFh. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. Byte 1FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells. The M48T58 includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T58 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

READ MODE

The M48T58 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E1}$ (Chip Enable 1) is low, and E2 (Chip Enable 2) is high. The unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E1}$, E2, and $\overline{G}$ access times are also satisfied. If the $\overline{E1}$, E2 and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Times (t_{E1LQV} or t_{E2HQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E1}$, E2 and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E1}$, E2 and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48T58 is in the Write Mode whenever $\overline{W}$ and $\overline{E1}$ are low and E2 is high. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E1}$, or the rising edge of E2. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E1}$, or the falling edge of E2. The addresses must be held valid throughout the cycle. $\overline{E1}$ or $\overline{W}$ must return high or E2 low for minimum of t_{E1HAX} or t_{E2LAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E1}$ and $\overline{G}$ and a high on E2, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48T58 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T58 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T58 for an accumulated period of at least 7 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues for t_{REC} until V_{CC} reaches V_{PFD}(min). $\overline{E1}$ should be kept high or E2 low as V_{CC} rises past V_{PFD}(min) to prevent inadvertent write cycles prior to processor stabilization. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max).

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, D6 in the Control register (1FF8h). As long as a '1' remains in that position, updating is halted.

After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0'.

Setting the Clock

Bit D7 of the Control register (1FF8h) is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 10). Resetting the WRITE bit to a '0' then transfers the values of all time registers (1FF9h-1FFFh) to the actual TIMEKEEPER counters and allows normal operation to resume. The FT bit and the bits marked as '0' in Table 10 must be written to '0' to allow for normal TIMEKEEPER and RAM operation. After the WRITE bit is reset, the next clock update will occur in one second.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T58 is shipped from SGS-THOMSON with the STOP bit set to a '1'. When reset to a '0', the M48T58 oscillator starts within 1 second.

Calibrating the Clock

The M48T58 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. With the calibration bits properly set, the accuracy of each M48T58 improves to better than ±4 PPM at 25°C.

Of course the oscillation rate of any crystal changes with temperature. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M48T58 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 9. The number of times pulses are blanked (subtracted, negative calibration) or

Table 10. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
1FFFh	10 Years				Year				Year	00-99
1FFEh	0	0	0	10 M.	Month				Month	01-12
1FFDh	0	0	10 Date		Date				Date	01-31
1FFCh	0	FT	0	0	0	Day			Day	01-07
1FFBh	0	0	10 Hours		Hours				Hour	00-23
1FFAh	0	10 Minutes			Minutes				Minutes	00-59
1FF9h	ST	10 Seconds			Seconds				Seconds	00-59
1FF8h	W	R	S	Calibration					Control	

Keys: **S** = SIGN Bit
FT = FREQUENCY TEST Bit (Must be set to '0' upon power, for normal clock operation)
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to '0'

split (added, positive calibration) depends upon the value loaded into the five Calibration bits found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits (D4-D0) in the Control register (1FF8h). These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or - 2.75 minutes per month.

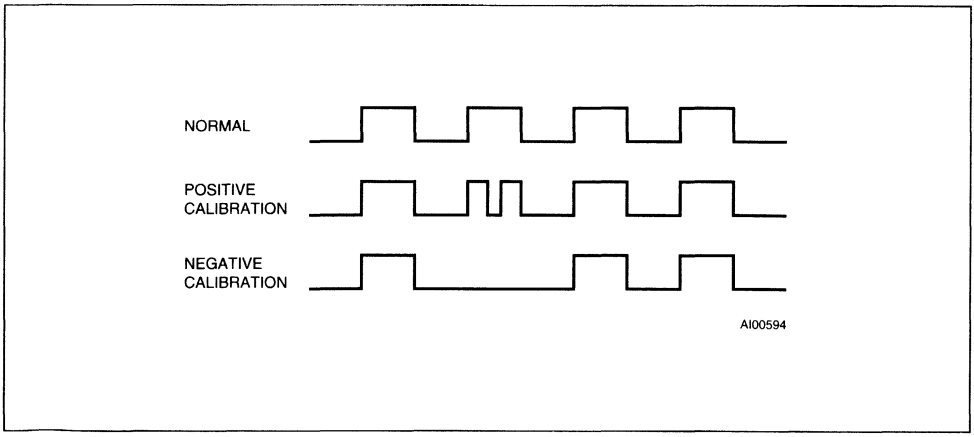
Two methods are available for ascertaining how much calibration a given M48T58 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day Register, is set to a '1', and the oscillator is running at 32,768 Hz, the Frequency Test (Pin 1) will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

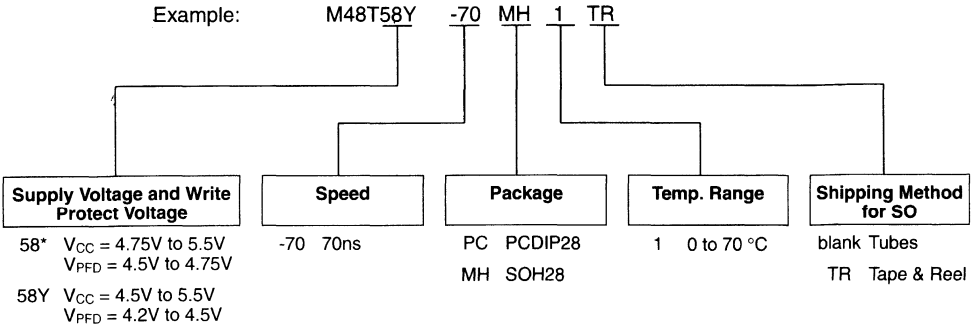
The FT bit must be set using the same method used to set the clock, using the Write bit.

The Frequency Test pin is an open drain output which requires a pull-up resistor for proper operation. A 500-10kΩ resistor is recommended in order to control the rise time.

Figure 9. Clock Calibration



ORDERING INFORMATION SCHEME



Note: 58* CAPHAT package only.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T28-BR12SH1".

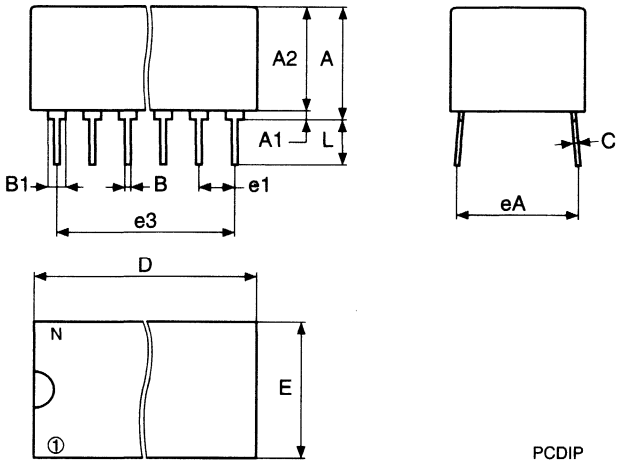
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP28 - 28 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

PCDIP28



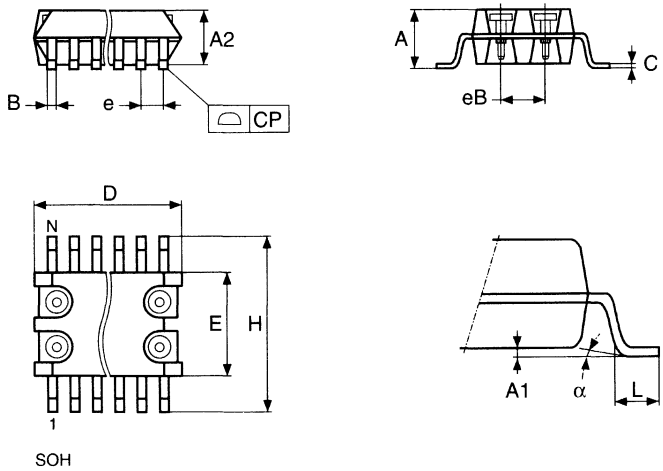
PCDIP

Drawing is not to scale

SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SOH28



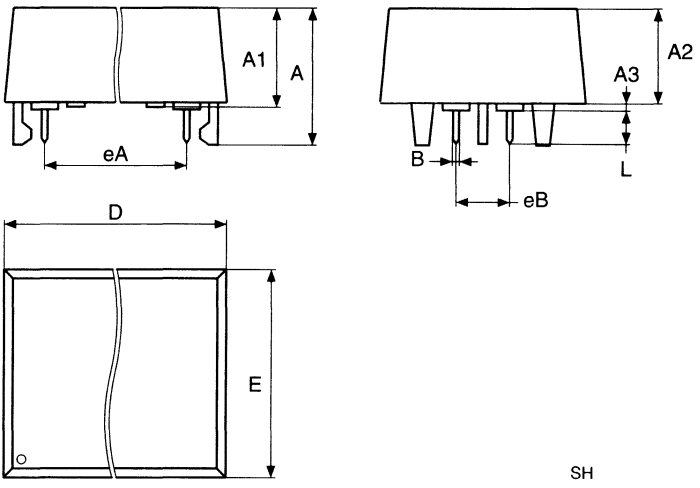
SOH

Drawing is not to scale

SH28 - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

SH28

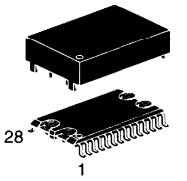


Drawing is not to scale

ADDRESS/DATA MULTIPLEXED 8K x 8 TIMEKEEPER SRAM

PRODUCT PREVIEW

- REGISTER COMPATIBLE with M48T58 and M48T18 TIMEKEEPER SRAM
- ADDREES/DATA MULTIPLEXED I/O PINS
- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT and BATTERY
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES and SECONDS
- FREQUENCY TEST OUTPUT for REAL TIME CLOCK
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGE:
  - M48T558Y: 4.2V ≤ V_{PFD} ≤ 4.5V
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY and CRYSTAL
- SNAPHAT HOUSING (BATTERY and CRYSTAL) REPLACEABLE



SOH28 (MH)
Battery SNAPHAT

DESCRIPTION

The M48T558 TIMEKEEPER™ RAM is an 8K x 8 non-volatile static RAM and real time clock. The monolithic chip is available in the SNAPHAT package to provide a highly integrated battery backed-up memory and real time clock solution.

Table 1. Signal Names

AD0-AD7	Address/Data
$\overline{AS0}$, $\overline{AS1}$	Address Strobes
$\overline{W}$	Write Enable
$\overline{R}$	Read Enable
$\overline{E}$	Chip Enable
FT	Frequency Test Output (Open Drain)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

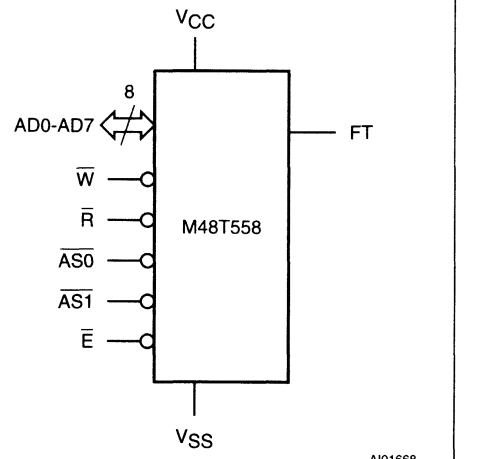
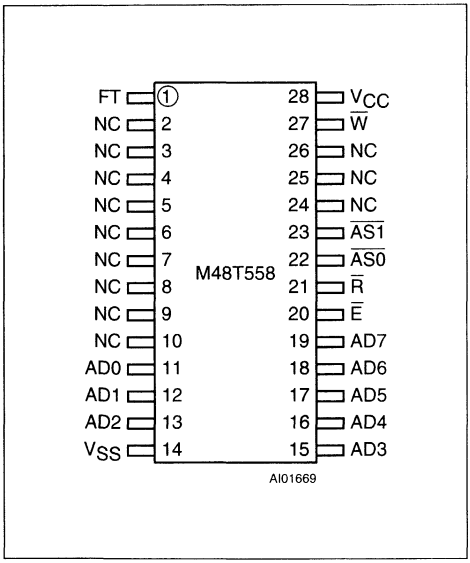


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Figure 2. SO Pin Connections



Warning: NC = Not Connected.

DESCRIPTION (cont'd)

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T28-BR12SH1".

As Figure 3 shows, the static memory array and the quartz controlled clock oscillator of the M48T558 are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 1FF8h-1FFFh. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. Byte 1FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells. The M48T558 includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

Figure 3. Block Diagram

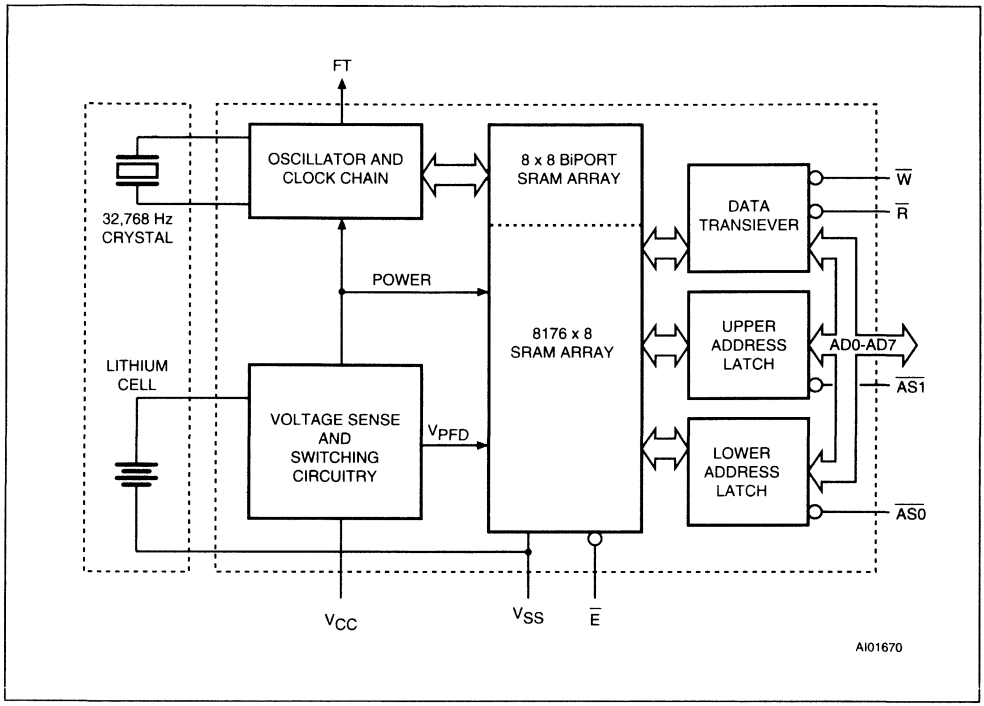


Table 3. Operating Modes (1)

Mode	V_{CC}	$\overline{E}$	$\overline{R}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min) (2)	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	High Z	Battery Back-up Mode

Notes: 1. X = V_{IH} or V_{IL}
2. See Table 6 for details..

The M48T558 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

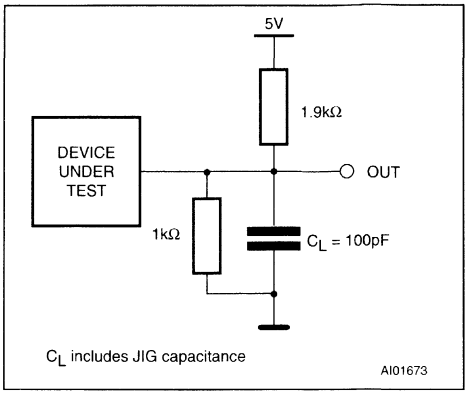


Table 4. Capacitance (1, 2) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} (3)	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} (1)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ = V_{CC} – 0.2V		3	mA
V_{IL} (2)	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
	Output Low Voltage (FT) (3)	I_{OL} = 10mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Notes: 1. Outputs Deselected.
2. Negative spikes of –1V allowed for up to 10ns once per cycle.
3. The FT pin is Open Drain.

Table 6. Power Down/Up Trip Points DC Characteristics (1) (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48T558Y)	4.2	4.35	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} (2)	Expected Data Retention Time	7			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	10		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	V_{PFD} (max) to Inputs Recognized	40	200	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

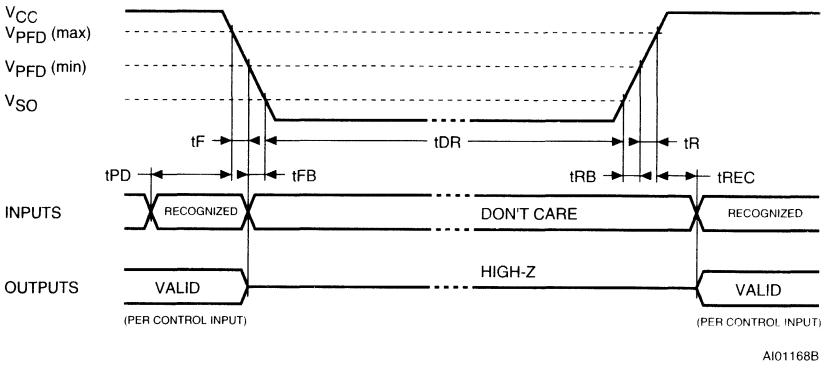
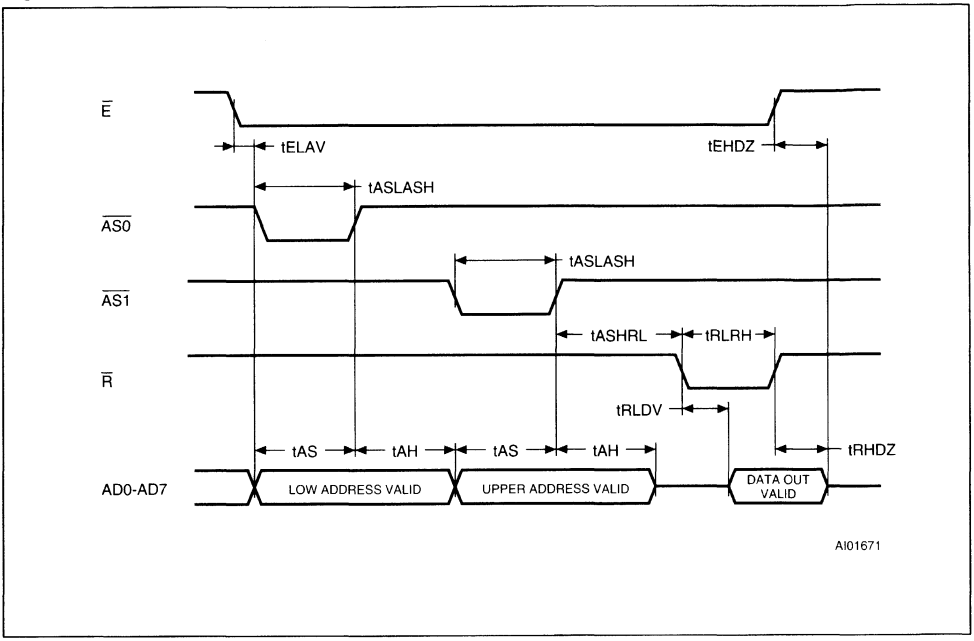
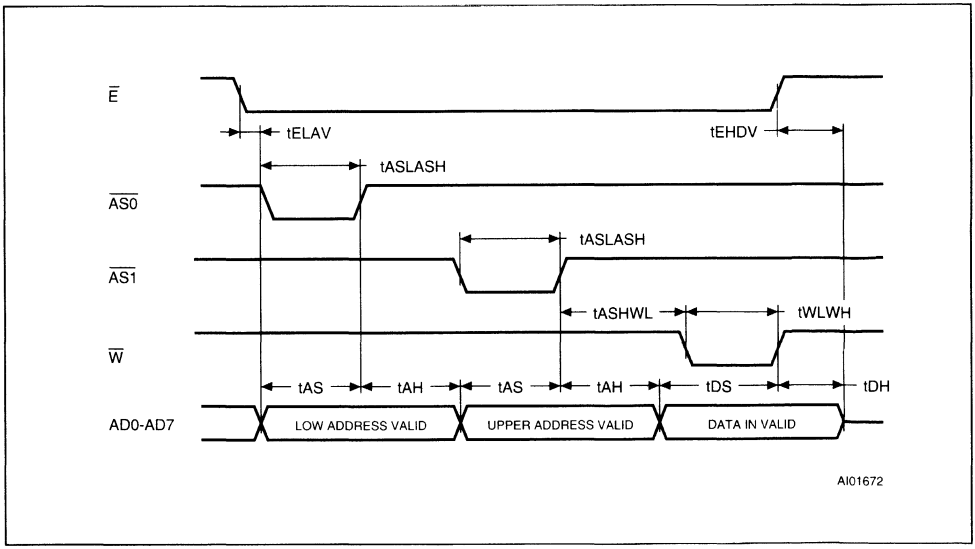


Figure 6. Read Mode AC Waveforms



Note: AD5-AD7 are don't care when latching upper address.

Figure 7. Write Mode AC Waveforms



Note: AD5-AD7 are don't care when latching upper address.

Table 8. AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	M48T558Y		Unit
		Min	Max	
t_{AS}	Address Setup Time	20		ns
t_{AH}	Address Hold Time	0		ns
t_{DS}	Data Setup Time	60		ns
t_{DH}	Data Hold Time	0		ns
t_{RLDV}	Read Enable Access Time		70	ns
t_{RLRH}	$\overline{R}$ Pulse Width Low	70		ns
t_{RHDZ}	Read Enable High to Output High Z		25	ns
t_{WLWH}	$\overline{W}$ Pulse Width Low	50		ns
t_{ASLASH}	$\overline{AS0}$, $\overline{AS1}$ Pulse Width Low	15		ns
t_{ASHRL}	$\overline{AS0}$, $\overline{AS1}$ High to $\overline{R}$ Low	15		ns
t_{ASHWL}	$\overline{AS0}$, $\overline{AS1}$ High to $\overline{W}$ Low	15		ns
t_{ELAV}	Chip Enable Low to Address Valid			ns
t_{EHDZ}	CHip Enable High to Data Output Hi-Z			ns
t_{EHDV}	Chip Enable High to Data Valid			ns

RAM OPERATION

Four control signals, $\overline{AS0}$, $\overline{AS1}$, $\overline{R}$ and $\overline{W}$, are used to access the M48T558. The address latches are loaded from the address/data bus in response to rising edge signals applied to the Address Strobe 0 ($\overline{AS0}$) and Address Strobe 1 ($\overline{AS1}$) signals. $\overline{AS0}$ is used to latch the lower 8 bits of address, and $\overline{AS1}$ is used to latch the upper 5 bits of address. It is necessary to meet the set-up and hold times given in the AC specifications with valid address information in order to properly latch the address. If the upper and/or lower order addresses are correct from a prior cycle, it is not necessary to repeat the address latching sequence.

A write operation reqires valid data to be placed on the bus (AD0-AD7) followed by the activation of the Write Enable ($\overline{W}$) line. Data on the bus will be written to the RAM provided that the write timing specifications are met. During a read cycle, the Read Enable ($\overline{R}$) signal is driven active. Data from the RAM will become valid on the bus provided that the RAM read access timing specifications are met.

The $\overline{W}$ and $\overline{R}$ signals should never be active at the same time. In addition $\overline{E}$ must be active before any control line are recognized.

DATA RETENTION MODE

With valid V_{CC} applied, the M48T558 supports industry standard read and write operations. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T558 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T558 for an accumulated period of at least 7 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Deselect continues for t_{REC} after V_{CC} reaches V_{PFD}(max).

Table 9. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
1FFFh	10 Years				Year				Year	00-99
1FFEh	0	0	0	10 M.	Month				Month	01-12
1FFDh	0	0	10 Date		Date				Date	01-31
1FFCh	0	FT	0	0	0	Day			Day	01-07
1FFBh	0	0	10 Hours		Hours				Hour	00-23
1FFAh	0	10 Minutes			Minutes				Minutes	00-59
1FF9h	ST	10 Seconds			Seconds				Seconds	00-59
1FF8h	W	R	S	Calibration					Control	

Keys: **S** = SIGN Bit
FT = FREQUENCY TEST Bit (Must be set to '0' upon power, for normal clock operation)
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to '0'

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, D6 in the Control register (1FF8h). As long as a '1' remains in that position, updating is halted.

After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0'.

Setting the Clock

Bit D7 of the Control register (1FF8h) is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 9). Resetting the WRITE bit to a '0' then transfers the values of all time registers (1FF9h-1FFFh) to the actual TIMEKEEPER counters and allows normal operation to resume. The FT bit and the bits marked as '0' in Table 9 must be written to '0' to allow for normal TIMEKEEPER and RAM operation. After the WRITE bit is reset, the next clock update will occur in one second.

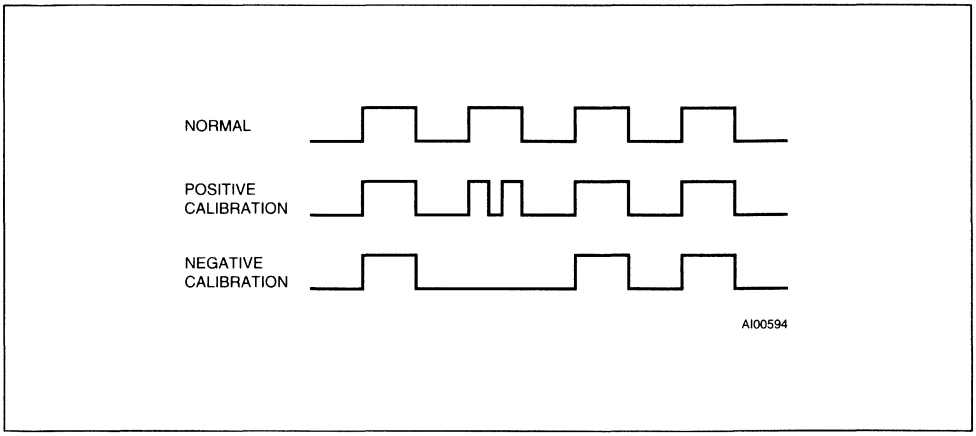
Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T558 is shipped from SGS-THOMSON with the STOP bit set to a '1'. When reset to a '0', the M48T558 oscillator starts within 1 second.

Calibrating the Clock

The M48T558 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. With the calibration bits properly set, the accuracy of each M48T558 improves to better than ±4 PPM at 25°C.

Figure 9. Clock Calibration



Of course the oscillation rate of any crystal changes with temperature. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M48T558 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 9. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five Calibration bits found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits (D4-D0) in the Control register (1FF8h). These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or - 2.75 minutes per month.

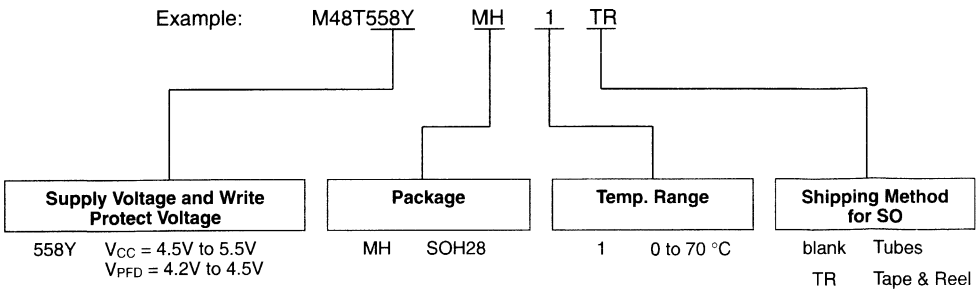
Two methods are available for ascertaining how much calibration a given M48T558 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day Register, is set to a '1', and the oscillator is running at 32,768 Hz, the Frequency Test (Pin 1) will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

The FT bit must be set using the same method used to set the clock, using the Write bit.

The Frequency Test pin is an open drain output which requires a pull-up resistor for proper operation. A 500-10kΩ resistor is recommended in order to control the rise time.

ORDERING INFORMATION SCHEME



The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T28-BR12SH1".

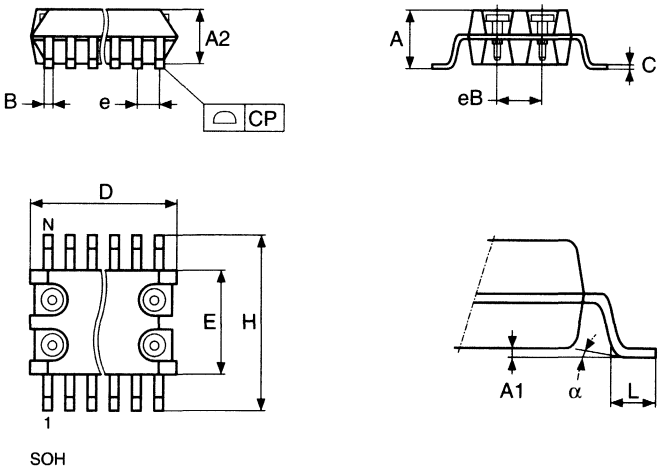
For a list of available options (Supply Voltage, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SOH28



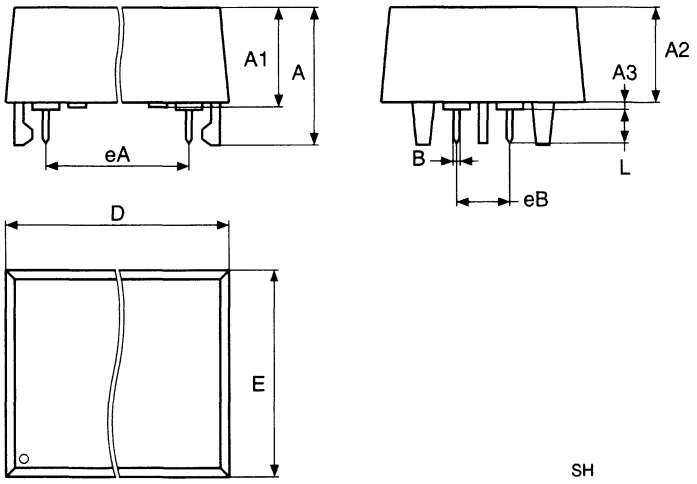
SOH

Drawing is not to scale

SH28 - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

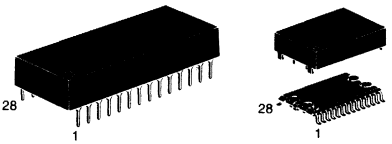
SH28



Drawing is not to scale

CMOS 8K x 8 TIMEKEEPER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT and BATTERY
- FREQUENCY TEST OUTPUT for REAL TIME CLOCK
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48T59: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48T59Y: 4.2V ≤ V_{PFD} ≤ 4.5V
- SELF CONTAINED BATTERY and CRYSTAL in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY and CRYSTAL
- SNAPHAT HOUSING (BATTERY and CRYSTAL) REPLACEABLE
- MICROPROCESSOR POWER-ON RESET
- PROGRAMMABLE ALARM OUTPUT ACTIVE in the BATTERY BACK-UP MODE
- BATTERY LOW WARNING



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

Figure 1. Logic Diagram

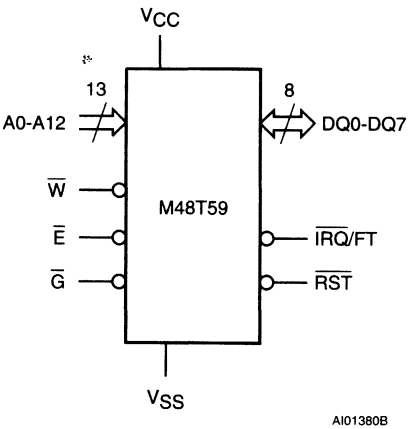


Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{IRQ}$/FT	Interrupt / Frequency Test Output (Open Drain)
$\overline{RST}$	Power Fail Reset Output (Open Drain)
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

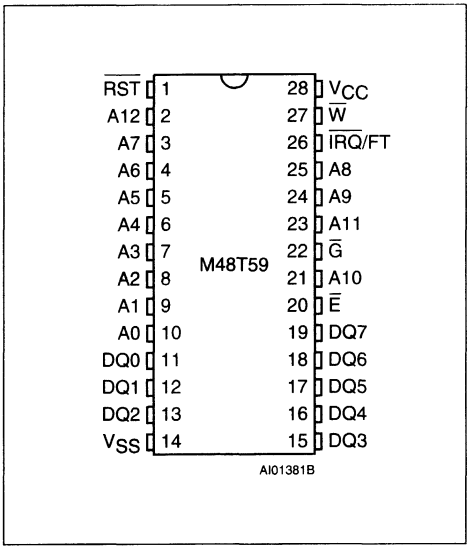


Figure 2B. SO Pin Connections

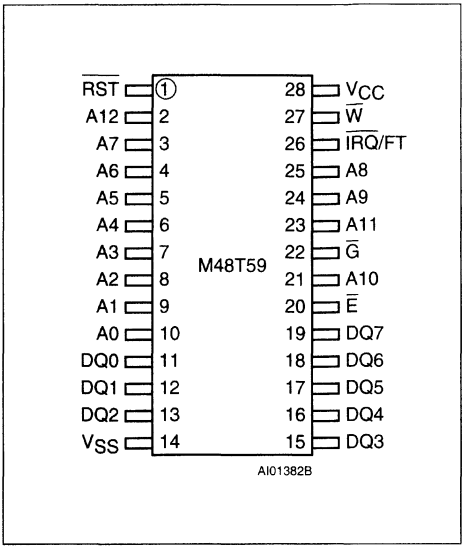


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

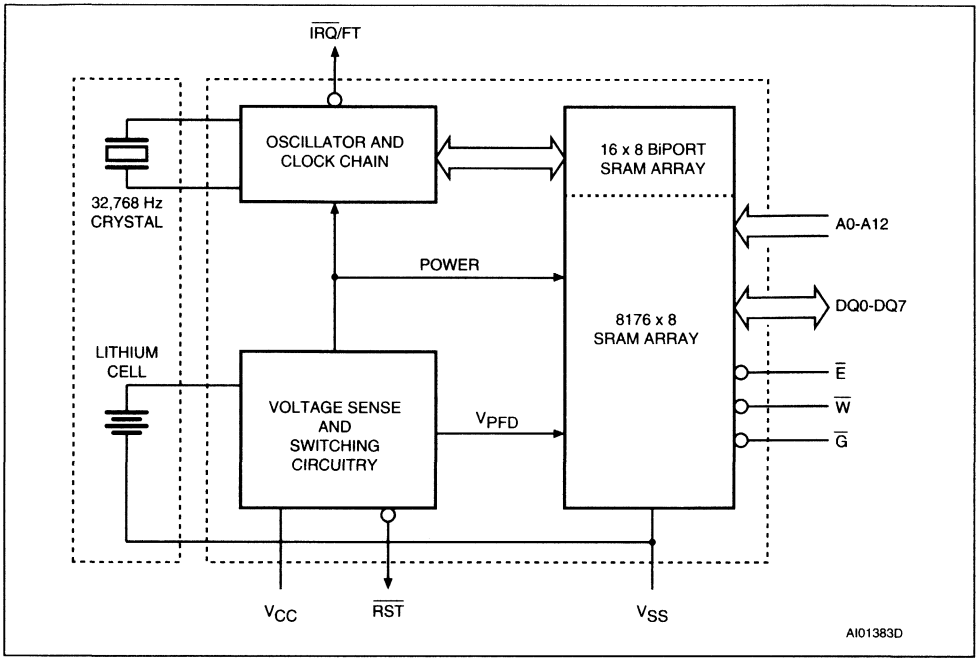
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes (1)

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min) (2)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	High Z	Battery Back-up Mode

Notes: 1. X = V_{IH} or V_{IL}
2. See Table 6 for details.

Figure 3. Block Diagram



DESCRIPTION

The M48T59 TIMEKEEPER™ RAM is an 8K x 8 non-volatile static RAM and real time clock. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory and real time clock solution.

The M48T59 is a non-volatile pin and function equivalent to any JEDEC standard 8K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 28 pin 600mil DIP CAPHAT™ houses the M48T59 silicon with a quartz crystal and a long life lithium button cell in a single package.

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

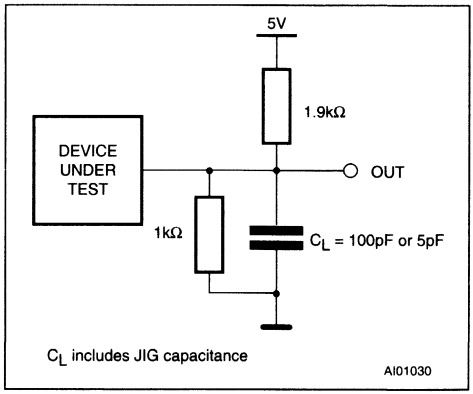


Table 4. Capacitance [1, 2] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [3]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO} [1]	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±5	µA
I_{CC}	Supply Current	Outputs open		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} - 0.2V$		3	mA
V_{IL} [2]	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
	Output Low Voltage ($\overline{IRQ}$/FT and $\overline{RST}$) [3]	I_{OL} = 10mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Notes: 1. Outputs Deselected.
2. Negative spikes of –1V allowed for up to 10ns once per Cycle.
3. The $\overline{IRQ}$/FT and $\overline{RST}$ pins are Open Drain.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48T59)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48T59Y)	4.2	4.35	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} [2]	Expected Data Retention Time	7			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

DESCRIPTION (cont'd)

to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T28-BR12SH1".

As Figure 3 shows, the static memory array and the quartz controlled clock oscillator of the M48T59 are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	10		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	V_{PFD} (max) to $\overline{RST}$ High	40	200	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

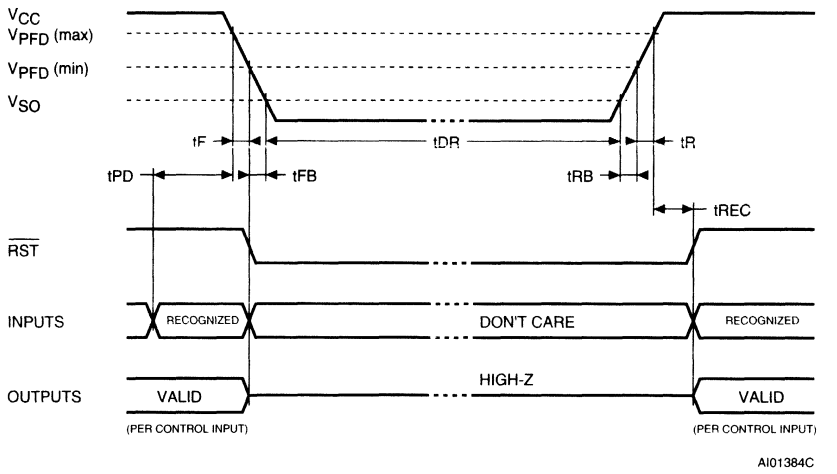
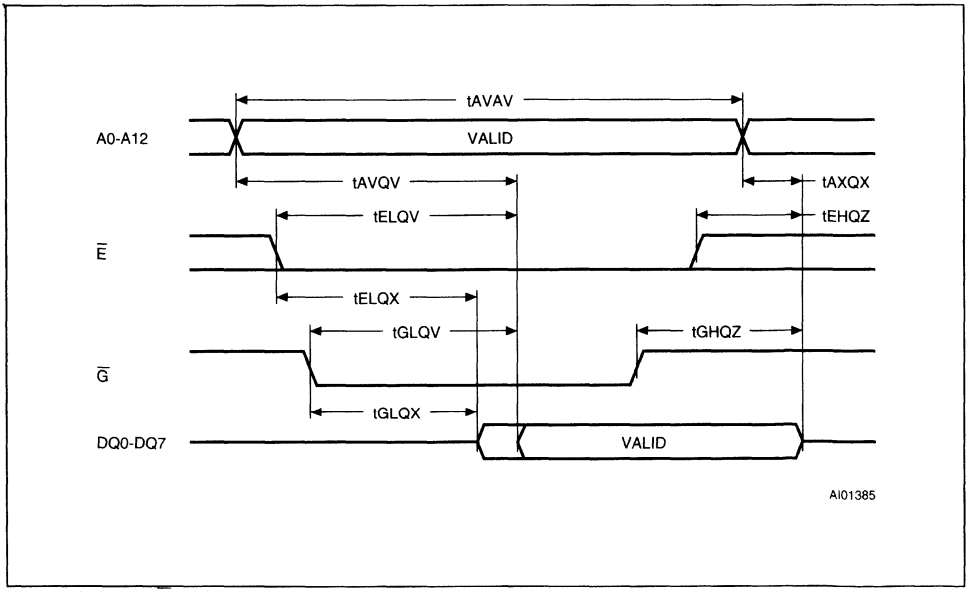


Table 8. Read Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48T59 / 59Y		Unit
		-70		
		Min	Max	
t_{AVAV}	Read Cycle Time	70		ns
t_{AVQV} (1)	Address Valid to Output Valid		70	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		70	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		35	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		25	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		ns

Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4).

Figure 6. Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High

Table 9. Write Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48T59 / 59Y		Unit
		-70		
		Min	Max	
t_{AVAV}	Write Cycle Time	70		ns
t_{AVWL}	Address Valid to Write Enable Low	0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		ns
t_{WLWH}	Write Enable Pulse Width	50		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	55		ns
t_{WHAX}	Write Enable High to Address Transition	0		ns
t_{EHAX}	Chip Enable High to Address Transition	0		ns
t_{DVWH}	Input Valid to Write Enable High	30		ns
t_{DVEH}	Input Valid to Chip Enable High	30		ns
t_{WHDX}	Write Enable High to Input Transition	5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		ns
t_{WLQZ} (1, 2)	Write Enable Low to Output Hi-Z		25	ns
t_{AVWH}	Address Valid to Write Enable High	60		ns
t_{AVE1H}	Address Valid to Chip Enable High	60		ns
t_{WHQX} (1, 2)	Write Enable High to Output Transition	5		ns

Notes: 1. C_L = 5pF (see Figure 4).
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

DESCRIPTION (cont'd)

to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 1FF8h-1FFFh. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. Byte 1FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells.

The M48T59 includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T59 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

Figure 7. Write Enable Controlled, Write AC Waveforms

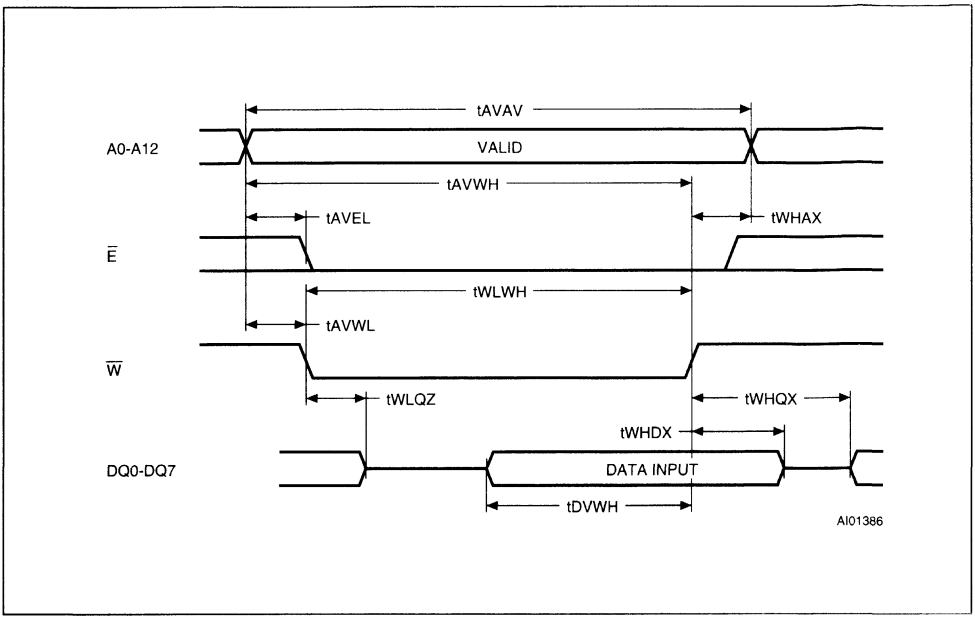
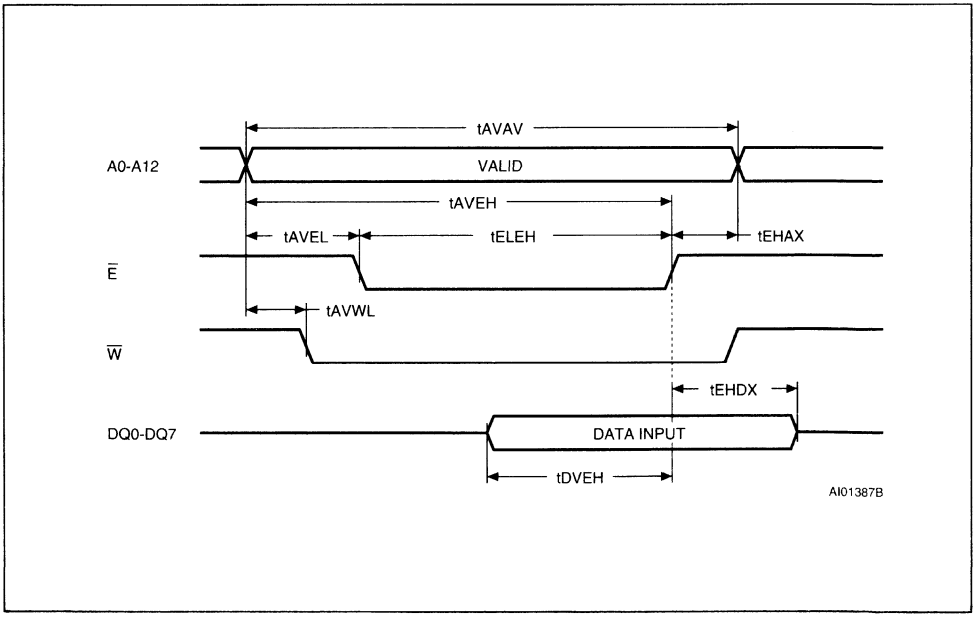


Figure 8. Chip Enable Controlled, Write AC Waveforms



READ MODE

The M48T59 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The unique address specified by the 13 Address Inputs defines which one of the 8,192 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48T59 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are low. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimumof t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$ a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48T59 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T59 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T59 for an accumulated period of at least 7 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Deselect continues for t_{REC} after V_{CC} reaches V_{PFD}(max).

POWER-ON RESET

The M48T59 continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ pulls low (open drain) and remains low on power-up for 40ms to 200ms after V_{CC} passes V_{PFD}. A 1kΩ resistor is recommended in order to control the rise time. The reset pulse remains active with V_{CC} at V_{SS}.

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, D6 in the Control register (1FF8h). As long as a '1' remains in that position, updating is halted.

After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0'.

Setting the Clock

Bit D7 of the Control register (1FF8h) is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 10). Resetting the WRITE bit to a '0' then transfers the values of all time registers (1FF9h-1FFFh) to the actual TIMEKEEPER counters and allows normal operation to resume. After the WRITE bit is reset, the next clock update will occur in one second.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T59 is shipped from SGS-THOMSON with the STOP bit set to a '1'. When reset to a '0', the M48T59 oscillator starts within 1 second.

Calibrating the Clock

The M48T59 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. With the calibration bits properly set, the accuracy of each M48T59 improves to better than ±4 PPM at 25°C.

Of course the oscillation rate of any crystal changes with temperature. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M48T59 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 9. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the

Table 10. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
1FFFh	10 Years				Year				Year	00-99
1FFEh	0	0	0	10 M.	Month				Month	01-12
1FFDh	0	0	10 Date		Date				Date	01-31
1FFCh	0	FT	0	0	0	Day			Day	01-07
1FFBh	0	0	10 Hours		Hours				Hour	00-23
1FFAh	0	10 Minutes			Minutes				Minutes	00-59
1FF9h	ST	10 Seconds			Seconds				Seconds	00-59
1FF8h	W	R	S	Calibration					Control	
1FF7h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
1FF6h	AFE	Y	ABE	Y	Y	Y	Y	Y	Interrupts	
1FF5h	RPT4	Y	Al. 10 Date		Alarm Date				Alarm Date	01-31
1FF4h	RPT3	Y	Al. 10 Hours		Alarm Hours				Alarm Hours	00-23
1FF3h	RPT2	Alarm 10 Minutes			Alarm Minutes				Alarm Minutes	00-59
1FF2h	RPT1	Alarm 10 Seconds			Alarm Seconds				Alarm Seconds	00-59
1FF1h	Y	Y	Y	Y	Y	Y	Y	Y	Unused	
1FF0h	WDF	AF	Z	BL	Z	Z	Z	Z	Flags	

Keys: **S** = SIGN Bit
FT = FREQUENCY TEST Bit
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to '0'
Y = '1' or '0'
Z = '0' and are Read only
AF = Alarm Flag
BL = Battery Low
WDS = Watchdog Steering Bit
BMB0-BMB4 = Watchdog Multiplier Bits
RB0-RB1 = Watchdog Resolution Bits
AFE = Alarm Flag Enable
ABE = Alarm in Battery Back-up Mode Enable
RPT1-RPT4 = Alarm Repeat Mode Bits
WDF = Watchdog Flag

value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits (D4-D0) in the Control register (1FF8h). These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or - 2.75 minutes per month.

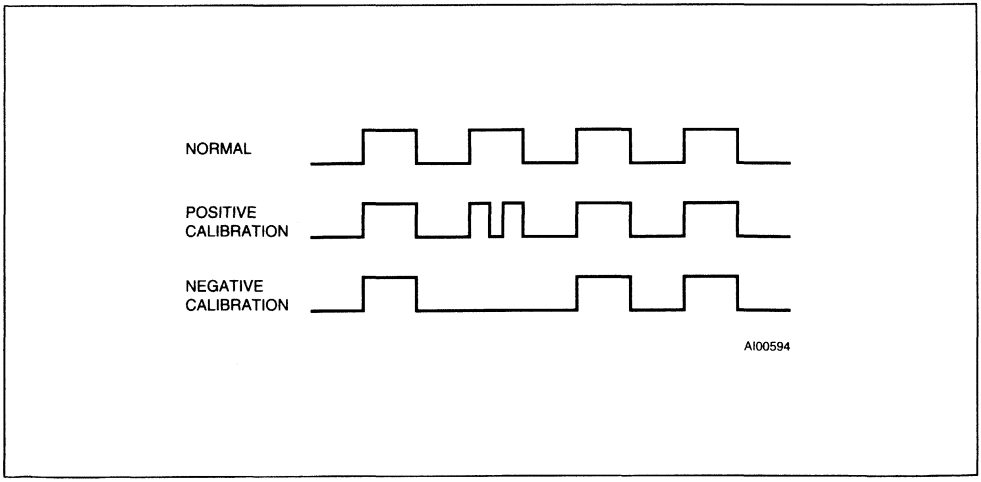
Two methods are available for ascertaining how much calibration a given M48T59 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{IRQ}$FT pin. The pin will toggle at 512Hz when the Stop bit (D7 of 1FF9h) is '0', the FT bit (D6 of 1FFCh) is '1', the AFE bit (D7 of 1FF6h) is '0', and the Watchdog Steering bit (D7 of 1FF7h) is '1' or the Watchdog Register is reset (1FF7h = 0).

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

The $\overline{IRQ}$/FT pin is an open drain output which requires a pull-up resistor for proper operation. A 500-10kΩ resistor is recommended in order to control the rise time. The FT bit is cleared on power-up.

Figure 9. Clock Calibration



SETTING ALARM CLOCK

Registers 1FF5h-1FF2h contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific day of the month or repeat every day, hour, minute, or second. It can also be programmed to go off while the M48T59 is in the battery back-up mode of operation to serve as a system wake-up call.

RPT1-RPT4 put the alarm in the repeat mode of operation. Table 11 shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT1-RPT4, AF (Alarm Flag) is set. If AFE (Alarm Flag Enable) is also set, the alarm condition activates the $\overline{IRQ}$/FT pin. The alarm flag and the $\overline{IRQ}$/FT output are cleared by a read to the Flags register as shown in Figure 10.

The $\overline{IRQ}$/FT pin can also be activated in the battery back-up mode. The $\overline{IRQ}$/FT will go low if an alarm occurs and both ABE (Alarm in Battery Back-up Mode Enable) and AFE are set. The ABE and AFE bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the Flag Register at system boot-up to determine if an alarm was generated while the M48T59 was in the deselect mode during power-up. Figure 11 illustrates the back-up mode alarm timing.

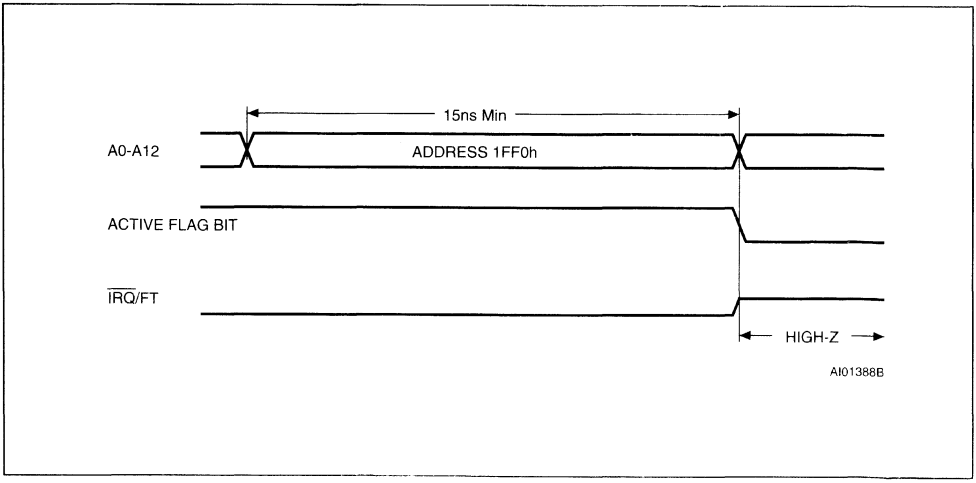
WATCHDOG TIMER

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the eight bit Watchdog Register (Address 1FF7h). The five bits (BMB4-BMB0) store a binary multiplier and the two lower order bits (RB1-RB0) select the resolution, where 00=1/16 second, 01=1/4 second, 10=1 second, and 11=4 seconds. The amount of time-out is then determined to be the multiplication of the five bit multiplier value with the resolution. (For example: writing 00001110 in the Watchdog Register = 3 x 1 or 3 seconds). If the processor does not reset the timer within the specified period, the M48T59 sets the WDF (Watchdog Flag) and generates a watchdog interrupt or a microprocessor reset.

Table 11. Alarm Repeat Mode

RPT4	RPT3	RPT2	RPT1	Alarm Activated
1	1	1	1	Once per Second
1	1	1	0	Once per Minute
1	1	0	0	Once per Hour
1	0	0	0	Once per Day
0	0	0	0	Once per Month

Figure 10. Interrupt Reset Waveforms



The most significant bit of the Watchdog Register is the Watchdog Steering Bit. When set to a '0', the watchdog will activate the $\overline{IRQ}$/FT pin when timed-out. When WDS is set to a '1', the watchdog will output a negative pulse on the $\overline{RST}$ pin for a duration of 40ms to 200ms. The Watchdog register and the FT bit will reset to a '0' at the end of a watchdog time-out when the WDS bit is set to a '1'.

The watchdog timer resets when the microprocessor performs a read of the Watchdog Register. The time-out period then starts over. The watchdog timer is disabled by writing a value of 00000000 to the eight bits in the Watchdog Register. The watchdog function is automatically disabled upon power-up and the Watchdog Register is cleared. If the watchdog function is set to output to the $\overline{IRQ}$/FT pin and the frequency test function is activated, the watchdog function prevails and the frequency test function is denied.

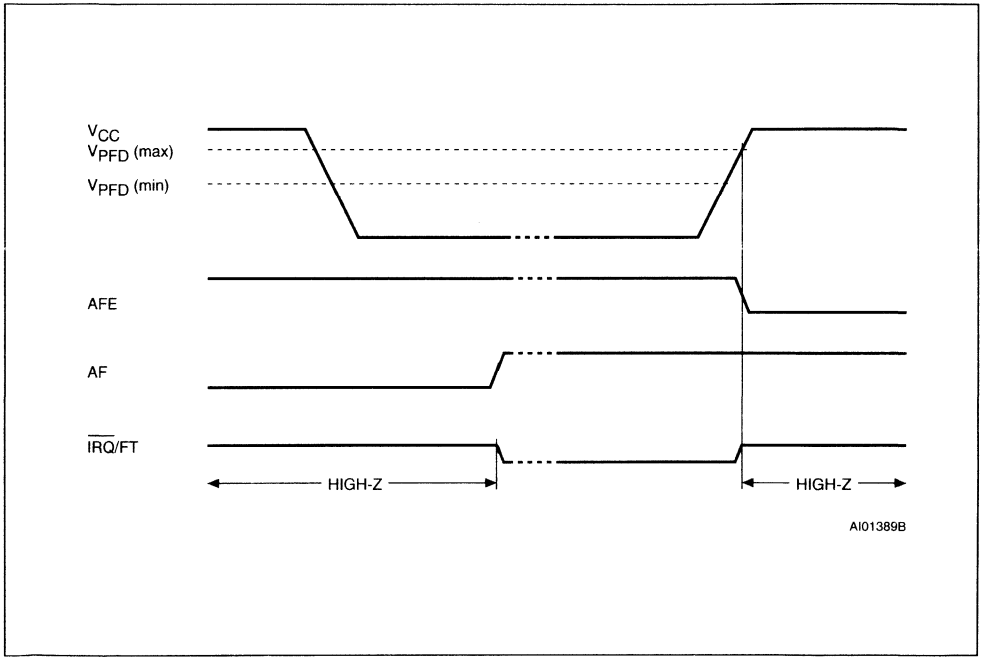
BATTERY LOW WARNING

The M48T59 checks it's battery voltage on power-up. The BL (Battery Low) bit (D4 of 1FF0h) will be set on power-up if the battery voltage is less than 2.5V (typical).

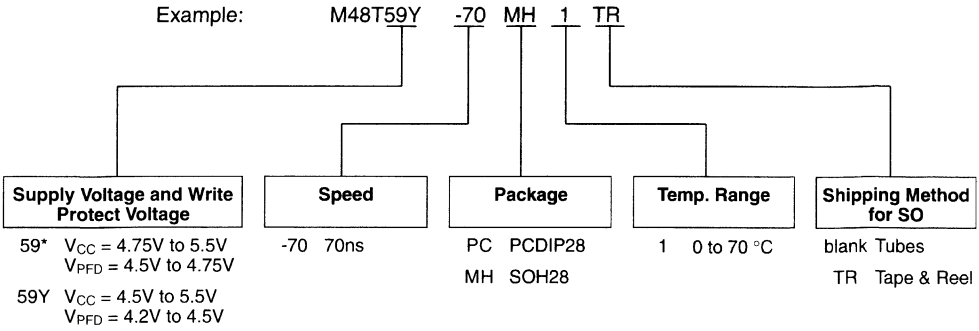
POWER-ON DEFAULTS

Upon application of power to the device, the following register bits are set to a '0' state: WDS = 0; BMB0-BMB4 = 0; RB0-RB1 = 0; AFE = 0; ABE = 0.

Figure 11. Back-up Mode Alarm Waveforms



ORDERING INFORMATION SCHEME



Note: 59* CAPHAT package only.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T28-BR12SH1".

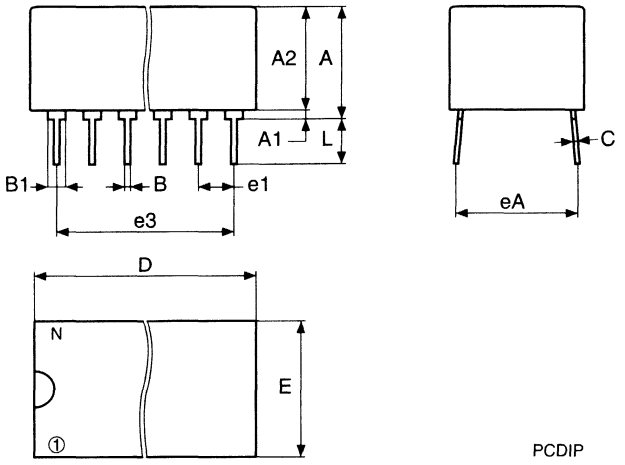
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP28 - 28 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N		28			28	

PCDIP28



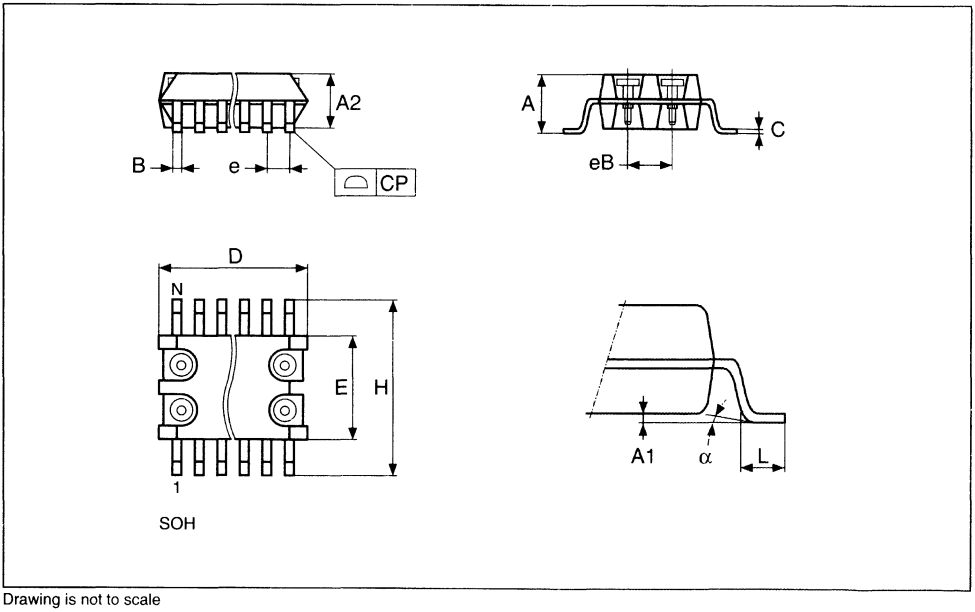
PCDIP

Drawing is not to scale

SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N		28			28	
CP			0.10			0.004

SOH28

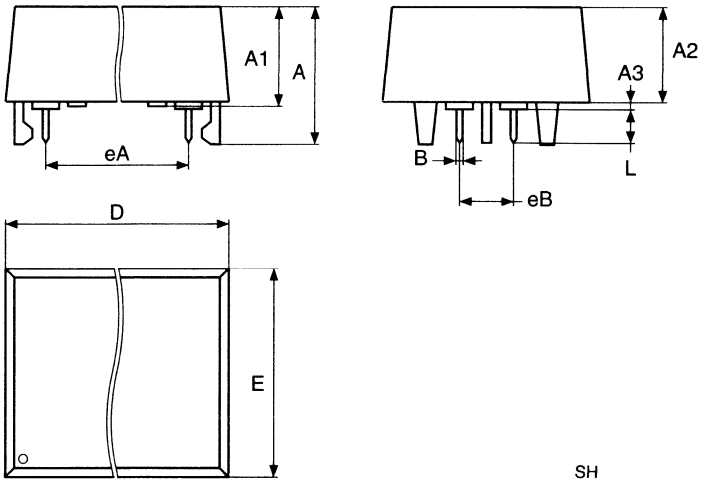


Drawing is not to scale

SH28 - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

SH28

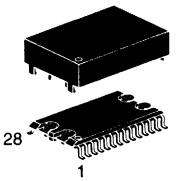


Drawing is not to scale

ADDRESS/DATA MULTIPLEXED 8K x 8 TIMEKEEPER SRAM

PRODUCT PREVIEW

- REGISTER COMPATIBLE with M48T59 TIMEKEEPER SRAM
- ADDREES/DATA MULTIPLEXED I/O PINS
- WATCHDOG TIMER - MONITORS OUT of CONTROL PROCESSOR or HUNG BUS
- ALARM with WAKE UP in BATTERY MODE
- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT and BATTERY
- FREQUENCY TEST OUTPUT for REAL TIME CLOCK
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGE:
  - M48T559Y: 4.2V ≤ V_{PFD} ≤ 4.5V
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY and CRYSTAL
- SNAPHAT HOUSING (BATTERY and CRYSTAL) REPLACEABLE
- MICROPROCESSOR POWER-ON RESET
- PROGRAMMABLE ALARM OUTPUT ACTIVE in the BATTERY BACK-UP MODE
- BATTERY LOW WARNING



SOH28 (MH)
Battery SNAPHAT

Table 1. Signal Names

AD0-AD7	Address/Data
$\overline{AS0}$-$\overline{AS1}$	Address Strobes
$\overline{W}$	Write Enable
$\overline{R}$	Read Enable
$\overline{E}$	Chip Enable
WDI	Watchdog Input
$\overline{RSTIN1}$-$\overline{RSTIN2}$	Reset Input
$\overline{RST}$	Power Fail Reset Output (Open Drain)
$\overline{IRQ}$	Interrupt Output (Open Drain)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

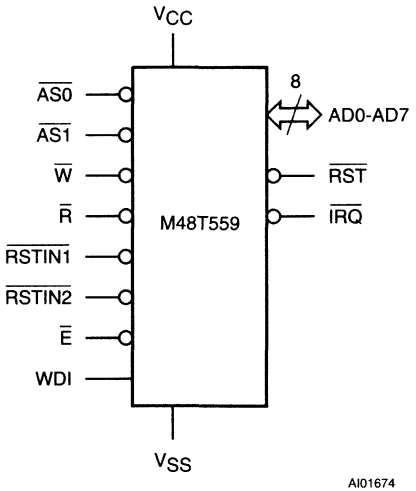
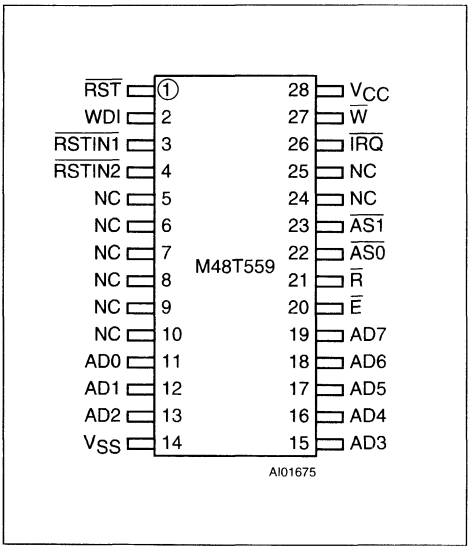


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Figure 2. SO Pin Connections



Warning: NC = Not Connected.

DESCRIPTION

The M48T559 TIMEKEEPER™ RAM is an 8K x 8 non-volatile static RAM and real time clock. The monolithic chip is available in the SNAPHAT package to provide a highly integrated battery backed-up memory and real time clock solution.

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T28-BR12SH1".

As Figure 3 shows, the static memory array and the quartz controlled clock oscillator of the M48T559 are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 1FF8h-1FFFh. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. Byte 1FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells. The M48T559 includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

Figure 3. Block Diagram

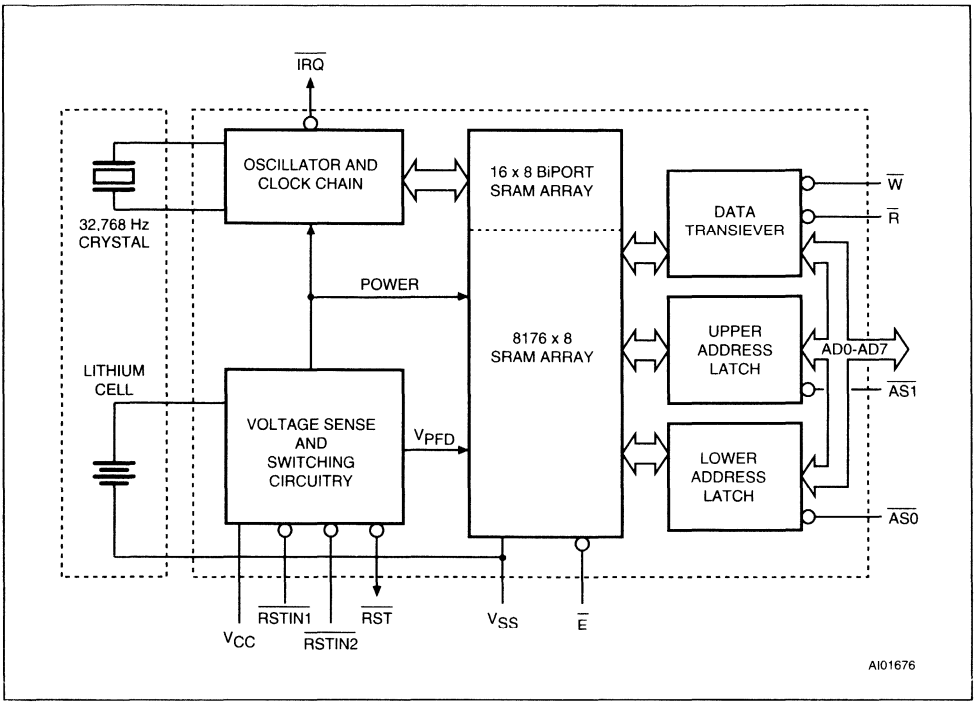


Table 3. Operating Modes (1)

Mode	V_{CC}	$\overline{E}$	$\overline{R}$	$\overline{W}$	AD0-AD7	Power
Deselect	4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min) (2)	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	High Z	Battery Back-up Mode

Notes: 1. X = V_{IH} or V_{IL}
2. See Table 6 for details.

The M48T559 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

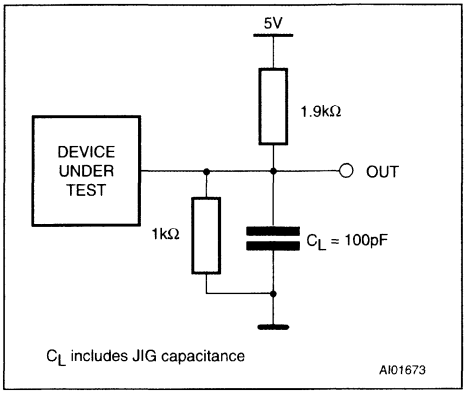


Table 4. Capacitance (1, 2) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} (3)	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} (1)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{LRST} (2)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		100	µA
I_{CC}	Supply Current	Outputs open		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ = V_{CC} – 0.2V		3	mA
V_{IL} (3)	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
	Output Low Voltage ($\overline{IRQ}$) (4)	I_{OL} = 10mA		0.4	V
V_{OH} (5)	Output High Voltage	I_{OH} = –1mA	2.4		V

Notes: 1. Outputs Deselected.
2. Input leakage current on input RESET pins.
3. Negative spikes of –1V allowed for up to 10ns once per Cycle.
4. The $\overline{IRQ}$ pin is Open Drain.
5. Measured with Control Bits set as follows: R = '1'; W, ST, FT = '0'.

Table 6. Power Down/Up Trip Points DC Characteristics (1) (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48T559Y)	4.2	4.35	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} (2)	Expected Data Retention Time	7			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	10		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	V_{PFD} (max) to $\overline{RST}$ High	40	200	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

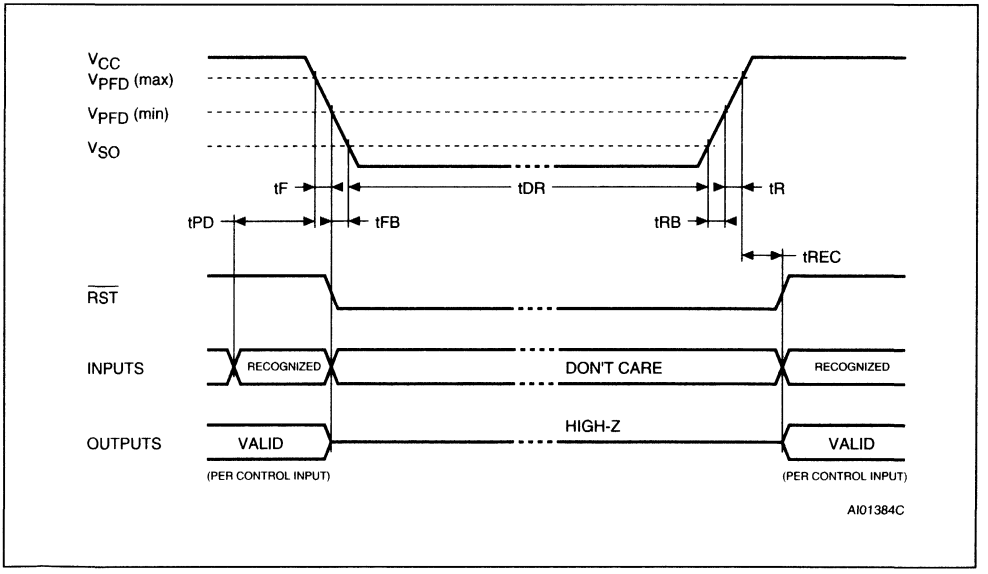
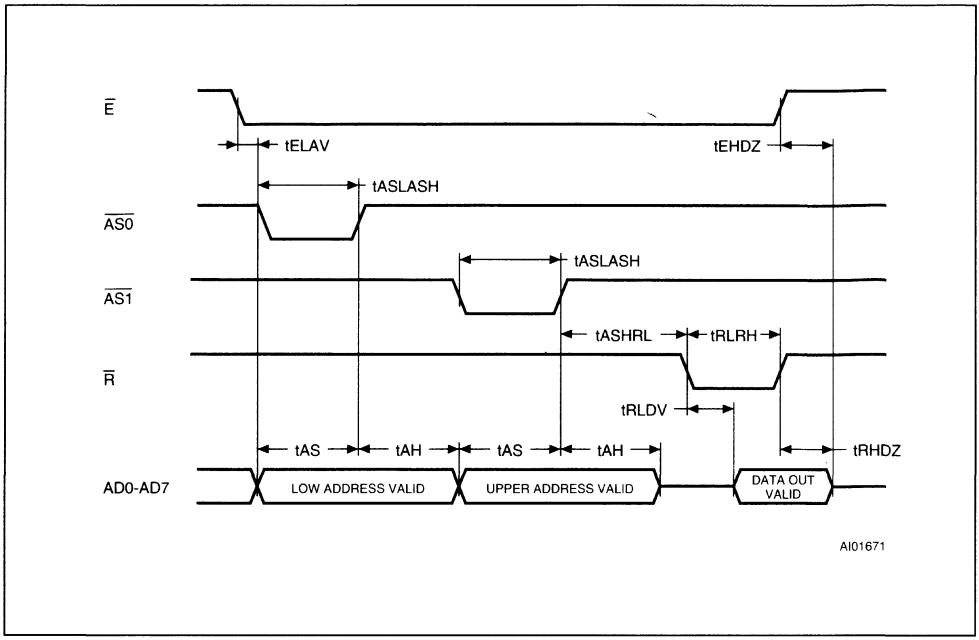
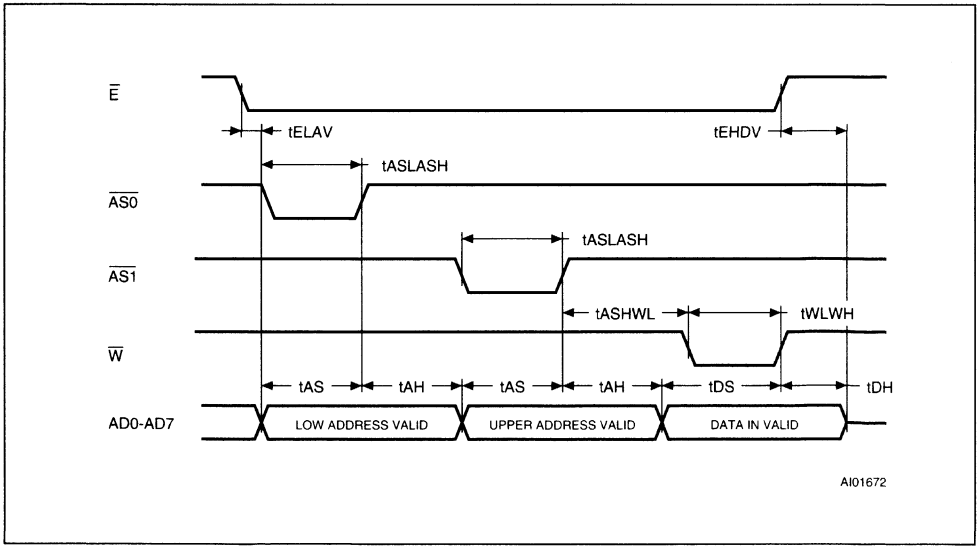


Figure 6. Read Mode AC Waveforms



Note: AD5-AD7 are don't care when latching upper address.

Figure 7. Write Mode AC Waveforms



Note: AD5-AD7 are don't care when latching upper address.

Table 8. AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	M48T559Y		Unit
		Min	Max	
t_{AS}	Address Setup Time	20		ns
t_{AH}	Address Hold Time	0		ns
t_{DS}	Data Setup Time	60		ns
t_{DH}	Data Hold Time	0		ns
t_{RLDV}	Read Enable Access Time		70	ns
t_{RLRH}	$\overline{R}$ Pulse Width Low	70		ns
t_{RHDZ}	Read Enable High to Output High Z		25	ns
t_{WLWH}	$\overline{W}$ Pulse Width Low	50		ns
t_{ASLASH}	$\overline{AS0}$, $\overline{AS1}$ Pulse Width Low	15		ns
t_{ASHRL}	$\overline{AS0}$, $\overline{AS1}$ High to $\overline{R}$ Low	15		ns
t_{ASHWL}	$\overline{AS0}$, $\overline{AS1}$ High to $\overline{W}$ Low	15		ns
t_{ELAV}	Chip Enable Low to Address Valid			ns
t_{EHDZ}	CHip Enable High to Data Output Hi-Z			ns
t_{EHDV}	Chip Enable High to Data Valid			ns

RAM OPERATION

Four control signals, $\overline{AS0}$, $\overline{AS1}$, $\overline{R}$ and $\overline{W}$, are used to access the M48T559. The address latches are loaded from the address/data bus in response to rising edge signals applied to the Address Strobe 0 ($\overline{AS0}$) and Address Strobe 1 ($\overline{AS1}$) signals. $\overline{AS0}$ is used to latch the lower 8 bits of address, and $\overline{AS1}$ is used to latch the upper 5 bits of address. It is necessary to meet the set-up and hold times given in the AC specifications with valid address information in order to properly latch the address. If the upper and/or lower order addresses are correct from a prior cycle, it is not necessary to repeat the address latching sequence.

A write operation reqires valid data to be placed on the bus (AD0-AD7) followed by the activation of the Write Enable ($\overline{W}$) line. Data on the bus will be written to the RAM provided that the write timing specifications are met. During a read cycle, the Read Enable ($\overline{R}$) signal is driven active. Data from the RAM will become valid on the bus provided that the RAM read access timing specifications are met.

The $\overline{W}$ and $\overline{R}$ signals should never be active at the same time. In addition $\overline{E}$ must be active before any control line are recognized.

INPUT RESET

The M48T559 provides two debounced inputs which can generate an output Reset. The duration and function of the Reset output is identical to a Reset generated by a power cycle. Pulses shorter than t_{R1} and t_{R2} will not generate a Reset condition.

DATA RETENTION MODE

With valid V_{CC} applied, the M48T559 supports industry standard read and write operations. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T559 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

Table 9. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
1FFFh	10 Years				Year				Year	00-99
1FFEh	0	0	0	10 M.	Month				Month	01-12
1FFDh	0	0	10 Date		Date				Date	01-31
1FFCh	0	FT	0	0	0	Day			Day	01-07
1FFBh	0	0	10 Hours		Hours				Hour	00-23
1FFAh	0	10 Minutes			Minutes				Minutes	00-59
1FF9h	ST	10 Seconds			Seconds				Seconds	00-59
1FF8h	W	R	S	Calibration					Control	
1FF7h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
1FF6h	AFE	Y	ABE	Y	Y	Y	Y	Y	Interrupts	
1FF5h	RPT4	Y	Al. 10 Date		Alarm Date				Alarm Date	01-31
1FF4h	RPT3	Y	Al. 10 Hours		Alarm Hours				Alarm Hours	00-23
1FF3h	RPT2	Alarm 10 Minutes			Alarm Minutes				Alarm Minutes	00-59
1FF2h	RPT1	Alarm 10 Seconds			Alarm Seconds				Alarm Seconds	00-59
1FF1h	Y	Y	Y	Y	Y	Y	Y	Y	Unused	
1FF0h	WDF	AF	Z	BL	Z	Z	Z	Z	Flags	

Keys: **S** = SIGN Bit
FT = FREQUENCY TEST Bit
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to '0'
Y = '1' or '0'
Z = '0' and are Read only
AF = Alarm Flag
BL = Battery Low
WDS = Watchdog Steering Bit
BMB0-BMB4 = Watchdog Multiplier Bits
RB0-RB1 = Watchdog Resolution Bits
AFE = Alarm Flag Enable
ABE = Alarm in Battery Back-up Mode Enable
RPT1-RPT4 = Alarm Repeat Mode Bits
WDF = Watchdog Flag

DATA RETENTION MODE (cont'd)

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T559 for an accumulated period of at least 7 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Deselect continues for t_{REC} after V_{CC} reaches V_{PFD}(max).

POWER-ON RESET

The M48T559 continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ pulls low (open drain) and remains low on power-up for 40ms to 200ms after V_{CC} passes V_{PFD}. A 1kΩ resistor is recommended in order to control the rise time. The reset pulse remains active with V_{CC} at V_{SS}.

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, D6 in the Control register (1FF8h). As long as a '1' remains in that position, updating is halted.

After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0'.

Setting the Clock

Bit D7 of the Control register (1FF8h) is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 9). Resetting the WRITE bit to a '0' then transfers the values of all time registers (1FF9h-1FFFh) to the actual TIMEKEEPER counters and allows normal operation to resume. After the WRITE bit is reset, the next clock update will occur in one second.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T559 is shipped from SGS-THOMSON with the STOP bit set to a '1'. When reset to a '0', the M48T559 oscillator starts within 1 second.

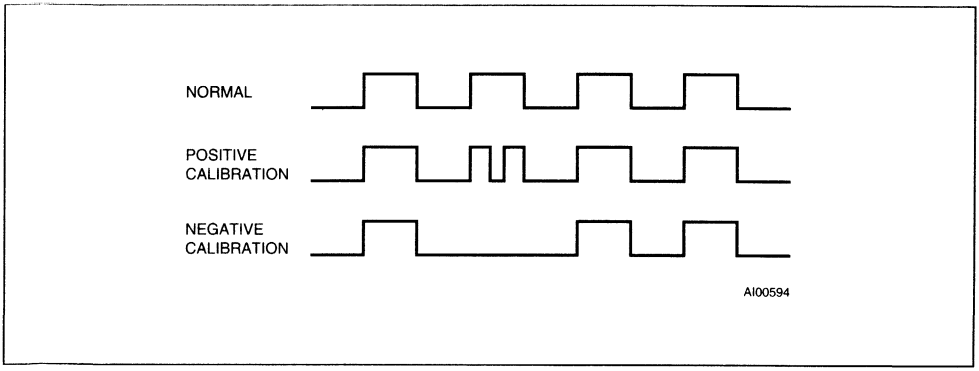
Calibrating the Clock

The M48T559 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. With the calibration bits properly set, the accuracy of each M48T559 improves to better than ±4 PPM at 25°C.

Of course the oscillation rate of any crystal changes with temperature. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M48T559 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 9. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits (D4-D0) in the Control register (1FF8h). These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles.

Figure 9. Clock Calibration



CLOCK OPERATIONS (cont'd)

If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or - 2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48T559 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{IRQ}$ pin. The pin will toggle at 512Hz when the Stop bit (D7 of 1FF9h) is '0', the FT bit (D6 of 1FFCh) is '1', the AFE bit (D7 of 1FF6h) is '0', and the Watchdog Steering bit (D7 of 1FF7h) is '1' or the Watchdog Register is reset (1FF7h = 0).

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

The $\overline{IRQ}$ pin is an open drain output which requires a pull-up resistor for proper operation. A 500-10kΩ resistor is recommended in order to control the rise time.

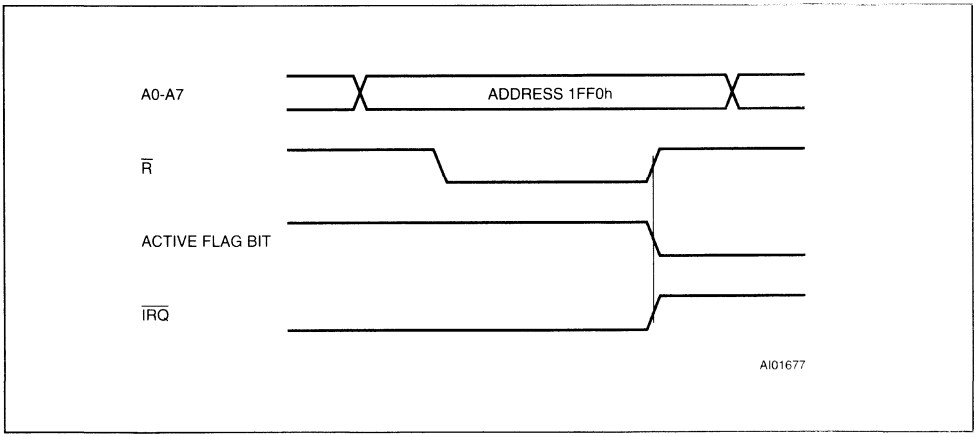
SETTING ALARM CLOCK

Registers 1FF5h-1FF2h contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific day of the month or repeat every day, hour, minute, or second. It can also be programmed to go off while the M48T559 is in the battery back-up mode of operation to serve as a system wake-up call.

Table 10. Alarm Repeat Mode

RPT4	RPT3	RPT2	RPT1	Alarm Activated
1	1	1	1	Once per Second
1	1	1	0	Once per Minute
1	1	0	0	Once per Hour
1	0	0	0	Once per Day
0	0	0	0	Once per Month

Figure 10. Interrupt Reset Waveforms



RPT1-RPT4 put the alarm in the repeat mode of operation. Table 11 shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT1-RPT4, AF (Alarm Flag) is set. If AFE (Alarm Flag Enable) is also set, the alarm condition activates the $\overline{IRQ}$ pin. The alarm flag and the $\overline{IRQ}$ output are cleared by a read to the Flags register as shown in Figure 10.

The $\overline{IRQ}$ pin can also be activated in the battery back-up mode. The $\overline{IRQ}$ will go low if an alarm occurs and both ABE (Alarm in Battery Back-up Mode Enable) and AFE are set. The ABE and AFE bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the Flag Register at system boot-up to determine if an alarm was generated while the M48T559 was in the deselect mode during power-up. Figure 11 illustrates the back-up mode alarm timing.

WATCHDOG TIMER

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the eight bit Watchdog Register (Address 1FF7h). The five bits (BMB4-BMB0) store a binary multiplier and the two lower order bits (RB1-RB0) select the resolution, where 00=1/16 second, 01=1/4 second, 10=1 second, and 11=4 seconds. The amount of time-out is then determined to be the multiplication of the five bit multiplier value with the resolution. (For example: writing 00001110 in the Watchdog Register = 3 x 1 or 3 seconds). If the processor does not reset the timer within the specified period, the M48T559 sets the WDF (Watchdog Flag) and generates a watchdog interrupt or a microprocessor reset.

The most significant bit of the Watchdog Register is the Watchdog Steering Bit. When set to a '0', the watchdog will activate the $\overline{IRQ}$ pin when timed-out. When WDS is set to a '1', the watchdog will output a negative pulse on the $\overline{RST}$ pin for a duration of 40ms to 200ms. The Watchdog register will resets to a '0' at the end of a watchdog time-out when the WDS bit is set to a '1'.

Figure 11. Back-up Mode Alarm Waveforms

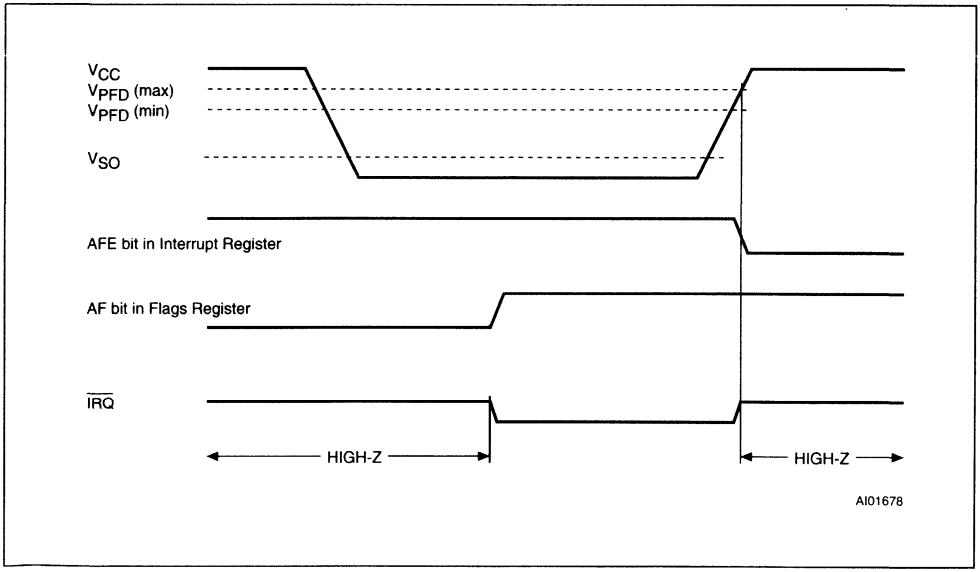


Figure 12. Reset Timing Waveforms

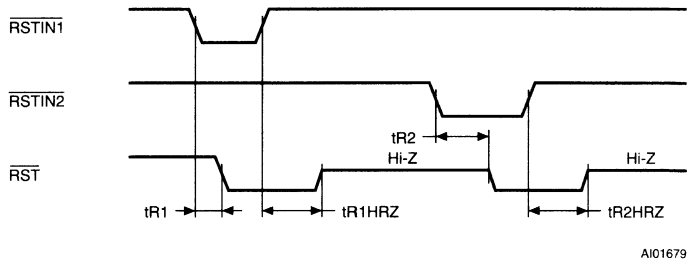


Table 11. Reset AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Min	Max	Unit
t_{R1}	$\overline{RSTIN1}$ Low to $\overline{RST}$ Low	50	200	ns
t_{R2}	$\overline{RSTIN2}$ Low to $\overline{RST}$ Low	20	100	ms
t_{R1HRZ}	$\overline{RSTIN1}$ High to $\overline{RST}$ Hi-Z	40	200	ms
t_{R2HRZ}	$\overline{RSTIN2}$ High to $\overline{RST}$ Hi-Z	40	200	ms

WATCHDOG TIMER (cont'd)

The watchdog timer resets when the microprocessor performs a read of the Watchdog Register. The time-out period then starts over. The watchdog timer is disabled by writing a value of 00000000 to the eight bits in the Watchdog Register. The watchdog function is automatically disabled upon power-up and the Watchdog Register is cleared. If the watchdog function is set to output to the $\overline{IRQ}$ pin and the frequency test function is activated, the watchdog function prevails and the frequency test function is denied.

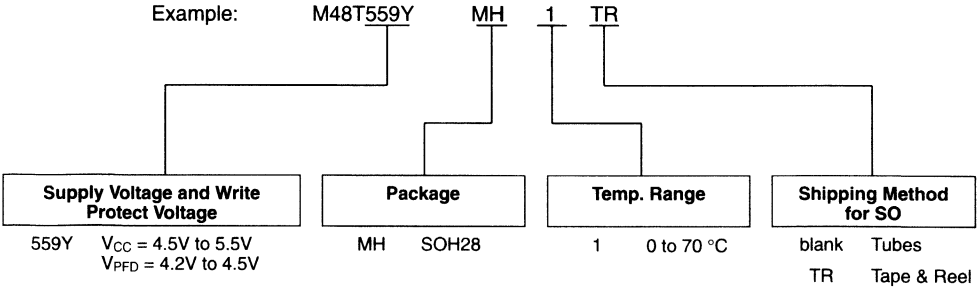
BATTERY LOW WARNING

The M48T559 checks it's battery voltage on power-up. The BL (Battery Low) bit (D4 of 1FF0h) will be set on power-up if the battery voltage is less than 2.5V (typical).

POWER-ON DEFAULTS

Upon application of power to the device, the following register bits are set to a '0' state: WDS = 0; BMB0-BMB4 = 0; RB0-RB1 = 0; AFE = 0; ABE = 0.

ORDERING INFORMATION SCHEME



The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T28-BR12SH1".

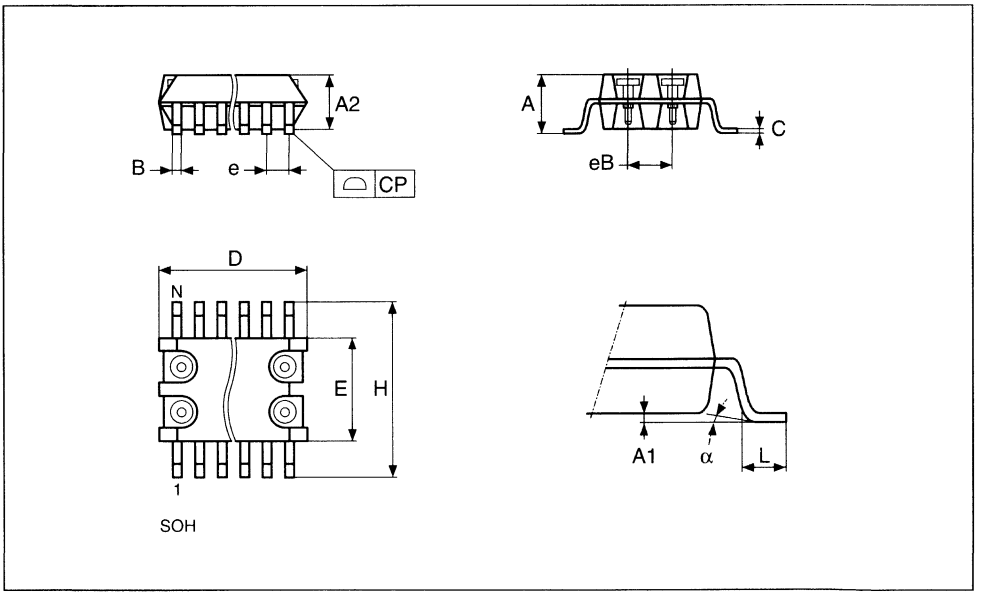
For a list of available options (Supply Voltage, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N		28			28	
CP			0.10			0.004

SOH28

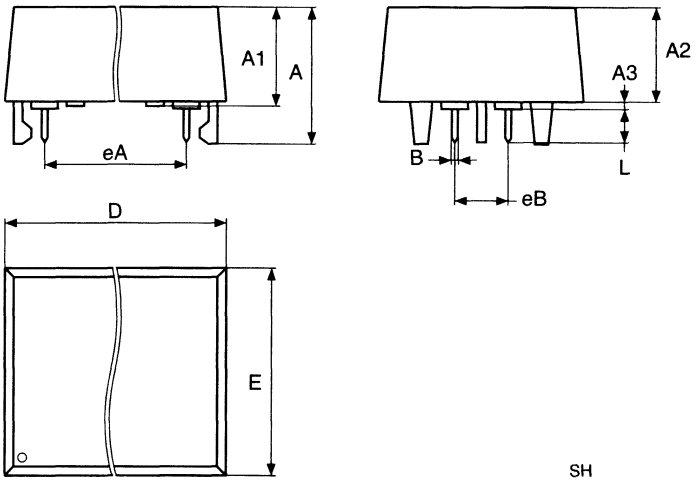


Drawing is not to scale

SH28 - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

SH28

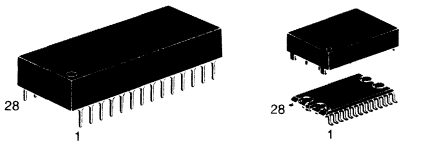


Drawing is not to scale

CMOS 32K x 8 TIMEKEEPER SRAM

PRELIMINARY DATA

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT and BATTERY
- BYTEWIDE RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES and SECONDS
- FREQUENCY TEST OUTPUT for REAL TIME CLOCK
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48T35: 4.5V ≤ V_{PFD} ≤ 4.75V
  - M48T35Y: 4.2V ≤ V_{PFD} ≤ 4.5V
- SELF CONTAINED BATTERY and CRYSTAL in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY and CRYSTAL
- SNAPHAT HOUSING (BATTERY and CRYSTAL) REPLACEABLE
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 32K x 8 SRAMs



PCDIP28 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

Figure 1. Logic Diagram

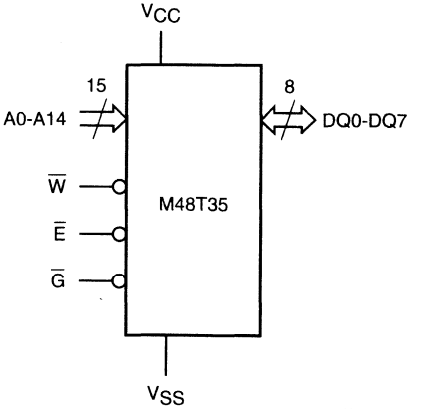


Table 1. Signal Names

A0-A14	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

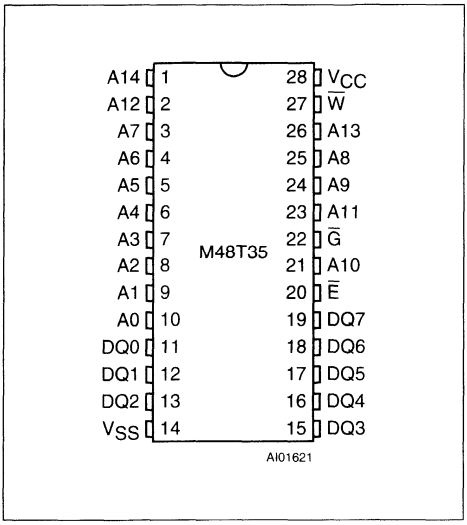


Figure 2B. SO Pin Connections

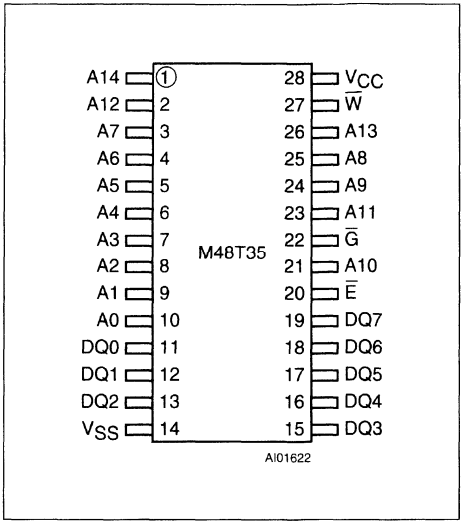


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

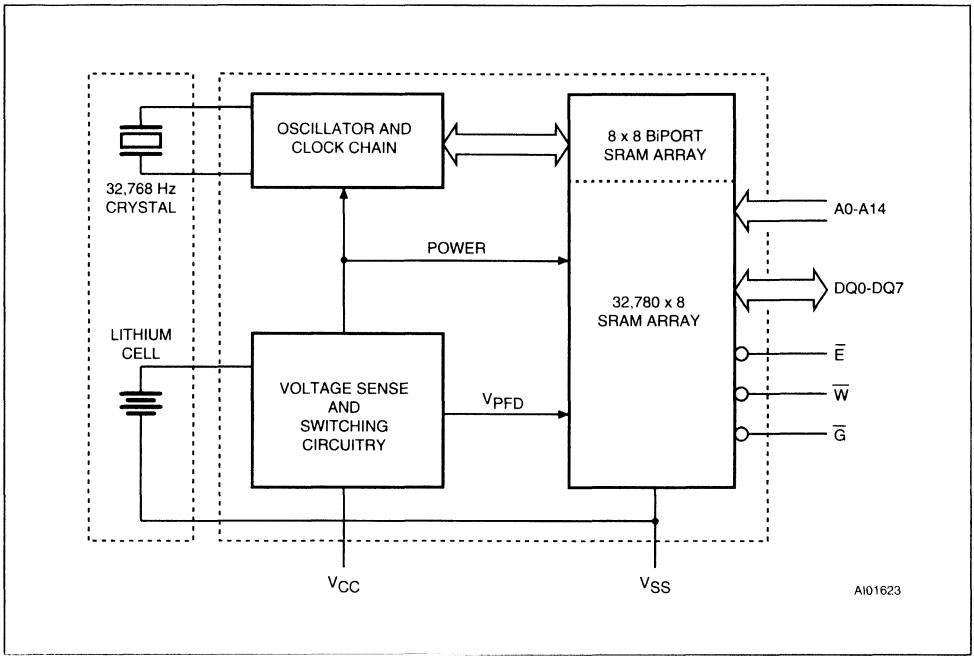
Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes (1)

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min) (2)	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	High Z	Battery Back-up Mode

Notes: 1. X = V_{IH} or V_{IL}
2. See Table 6 for details.

Figure 3. Block Diagram



DESCRIPTION

The M48T35 TIMEKEEPER™ RAM is an 32K x 8 non-volatile static RAM and real time clock. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory and real time clock solution.

The M48T35 is a non-volatile pin and function equivalent to any JEDEC standard 32K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 28 pin 600mil DIP CAPHAT™ houses the M48T35 silicon with a quartz crystal and a long life lithium button cell in a single package.

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

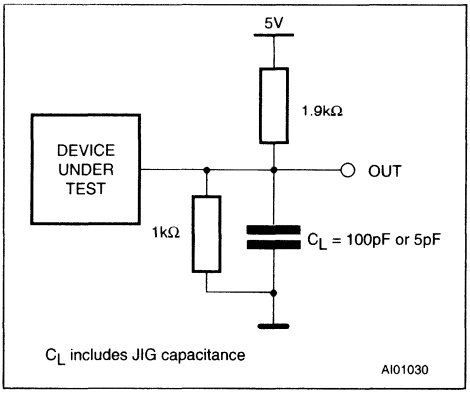


Table 4. Capacitance [1, 2] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [3]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} [1]	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ = V_{CC} – 0.2V		3	mA
V_{IL} [2]	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Notes: 1. Outputs Deselected.
2. Negative spikes of –1V allowed for up to 10ns once per Cycle.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48T35)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48T35Y)	4.2	4.35	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} [2, 3]	Expected Data Retention Time	10			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C.
3. CAPHAT only, SNAPHAT t_{DR} = 7yrs.

DESCRIPTION (cont'd)

to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T28-BR12SH1".

As Figure 3 shows, the static memory array and the quartz controlled clock oscillator of the M48T35 are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	10		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	V_{PFD}(max) to Inputs Recognized	40	200	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

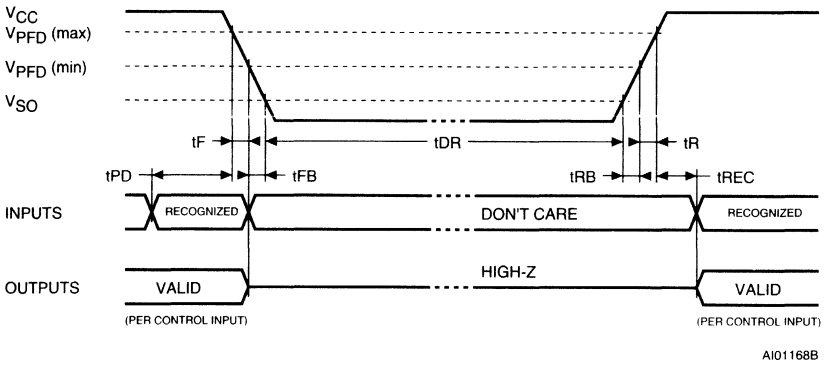
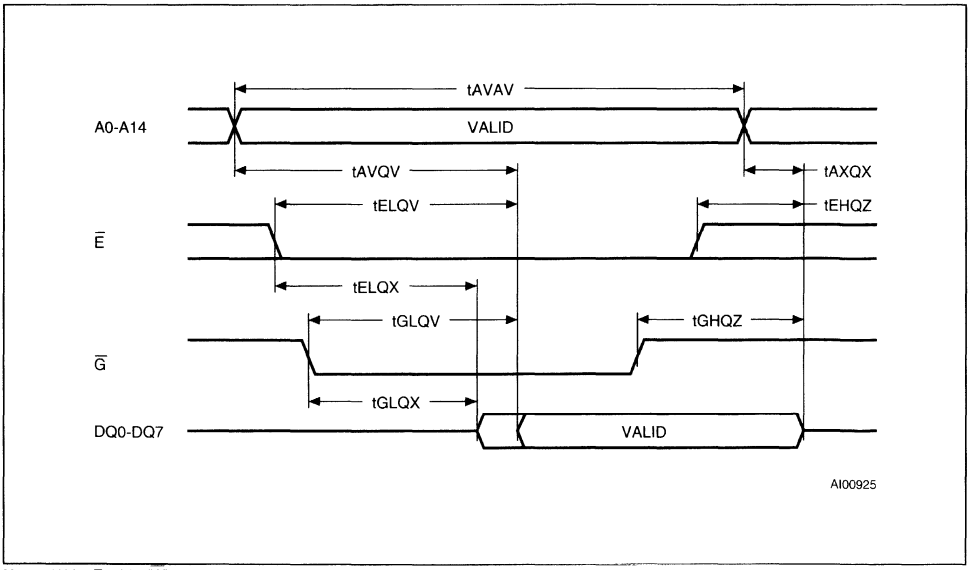


Table 8. Read Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48T35 / 35Y		Unit
		-70		
		Min	Max	
t_{AVAV}	Read Cycle Time	70		ns
t_{AVQV} (1)	Address Valid to Output Valid		70	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		70	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		35	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		25	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		ns

Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4).

Figure 6. Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High

Table 9. Write Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48T35 / 35Y		Unit
		-70		
		Min	Max	
t_{AVAV}	Write Cycle Time	70		ns
t_{AVWL}	Address Valid to Write Enable Low	0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		ns
t_{WLWH}	Write Enable Pulse Width	50		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	55		ns
t_{WHAX}	Write Enable High to Address Transition	0		ns
t_{EHAX}	Chip Enable High to Address Transition	0		ns
t_{DVWH}	Input Valid to Write Enable High	30		ns
t_{DVEH}	Input Valid to Chip Enable High	30		ns
t_{WHDX}	Write Enable High to Input Transition	5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		ns
t_{WLQZ} (1, 2)	Write Enable Low to Output Hi-Z		25	ns
t_{AVWH}	Address Valid to Write Enable High	60		ns
t_{AVEH}	Address Valid to Chip Enable High	60		ns
t_{WHQX} (1, 2)	Write Enable High to Output Transition	5		ns

Notes: 1. C_L = 5pF (see Figure 4).
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

DESCRIPTION (cont'd)

to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 7FF9h-7FFFh. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. Byte 7FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells. The M48T35 includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T35 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

READ MODE

The M48T35 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The unique address specified by the 15 Address Inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable,

Figure 7. Write Enable Controlled, Write AC Waveforms

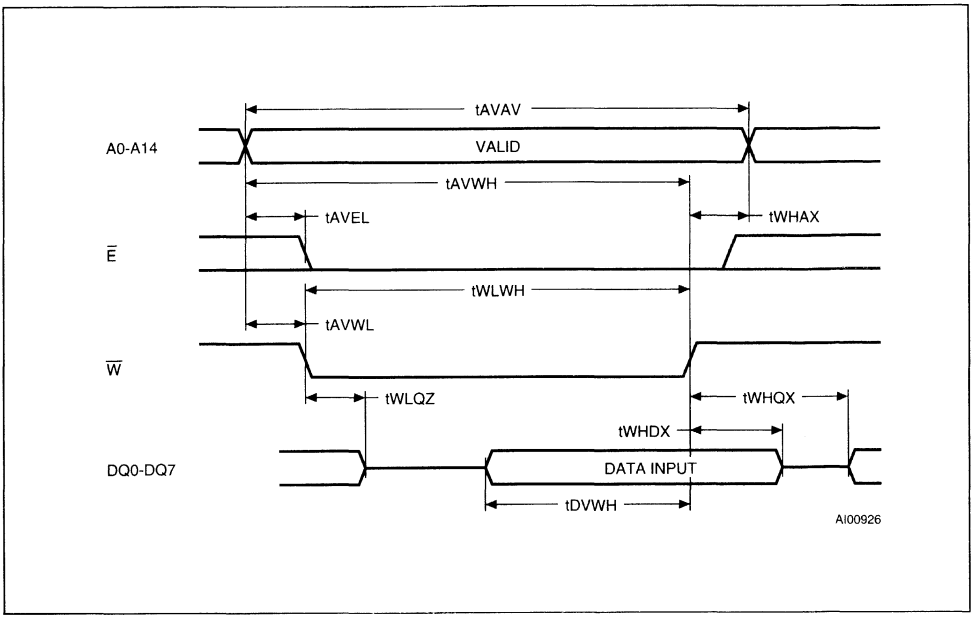
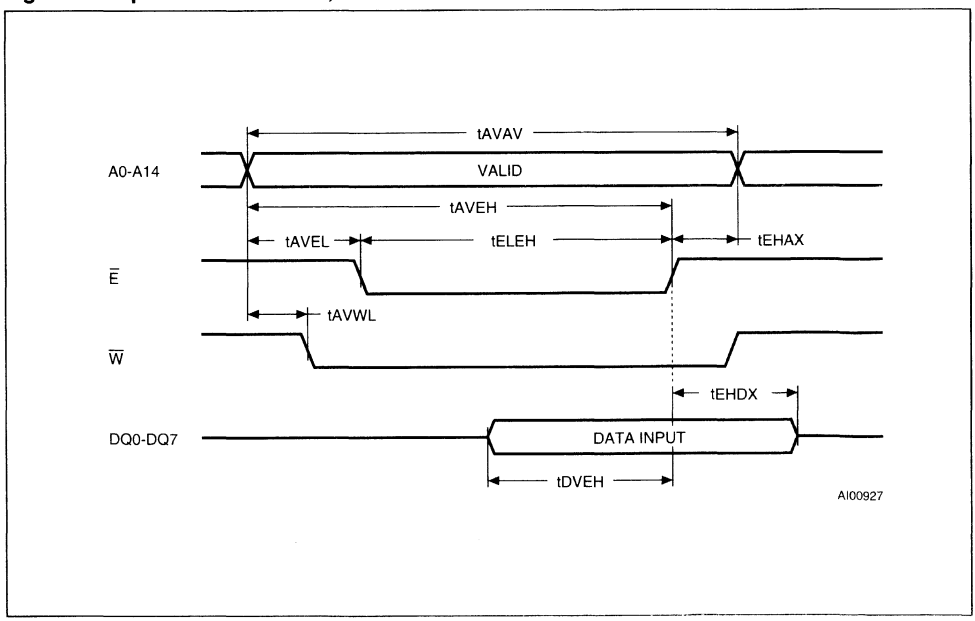


Figure 8. Chip Enable Controlled, Write AC Waveforms



RAED MODE (cont'd)

providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Times (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48T35 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are low. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48T35 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T35 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T35 for an accumulated period of at least 7 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues for t_{REC} until V_{CC} reaches V_{PFD}(min). $\overline{E}$ should be kept high as V_{CC} rises past V_{PFD}(min) to prevent inadvertent write cycles prior to processor stabilization. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max).

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, D6 in the Control Register 7FF8h. As long as a '1' remains in that position, updating is halted.

After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0'.

Setting the Clock

Bit D7 of the Control Register 7FF8h is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 10). Resetting the WRITE bit to a '0' then transfers the values of all time registers 7FF9h-7FFFh to the actual TIMEKEEPER counters and allows normal operation to resume. The FT bit and the bits marked as '0' in Table 10 must be written to '0' to allow for normal TIMEKEEPER and RAM operation. After the WRITE bit is reset, the next clock update will occur in one second.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T35 is shipped from SGS-THOMSON with the STOP bit set to a '1'. When reset to a '0', the M48T35 oscillator starts within 1 second.

Calibrating the Clock

The M48T35 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. With the calibration bits properly set, the accuracy of each M48T35 improves to better than ±4 PPM at 25°C.

Of course the oscillation rate of any crystal changes with temperature. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M48T35 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 9. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five Calibration bits found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits (D4-D0) in the Control Register 7FF8h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or - 2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48T35 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure.

All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

Table 10. Register Map

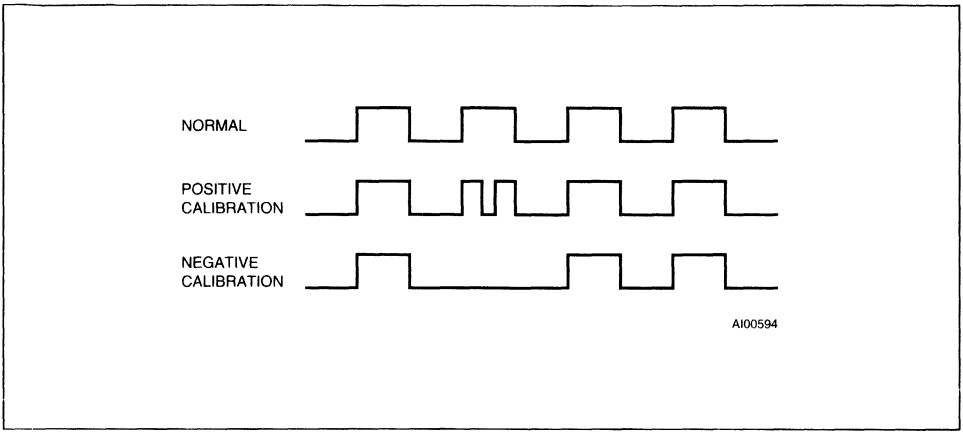
Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
7FFFh	10 Years				Year				Year	00-99
7FFEh	0	0	0	10 M.	Month				Month	01-12
7FFDh	0	0	10 Date		Date				Date	01-31
7FFCh	0	FT	0	0	0	Day			Day	01-07
7FFBh	0	0	10 Hours		Hours				Hour	00-23
7FFAh	0	10 Minutes			Minutes				Minutes	00-59
7FF9h	ST	10 Seconds			Seconds				Seconds	00-59
7FF8h	W	R	S	Calibration					Control	

Keys: **S** = SIGN Bit
FT = FREQUENCY TEST Bit (Must be set to '0' upon power, for normal clock operation)
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to '0'

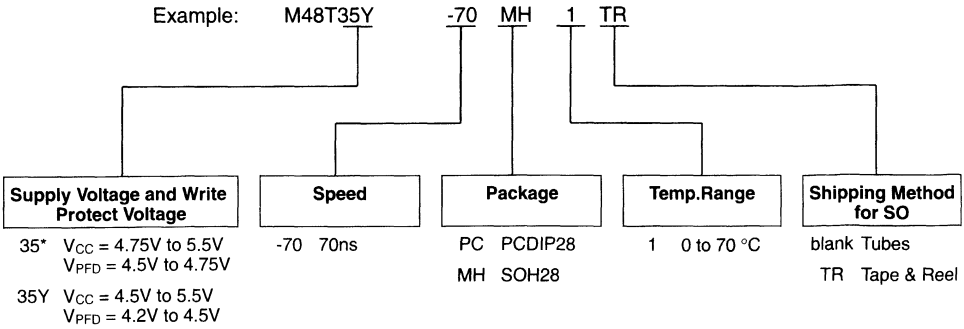
The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day Register is set to a '1', and D7 of the Seconds Register is a '0' (Oscillator Running), DQ0 will toggle at 512Hz during a read of the Seconds Register. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

The FT bit MUST be reset to '0' for normal clock operations to resume. The FT bit is automatically Reset on power-up.

Figure 9. Clock Calibration



ORDERING INFORMATION SCHEME



Note: 35* CAPHAT package only.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T28-BR12SH1".

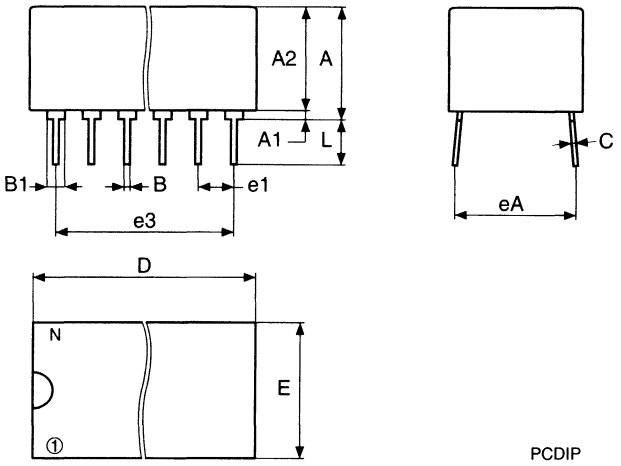
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP28 - 28 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

PCDIP28



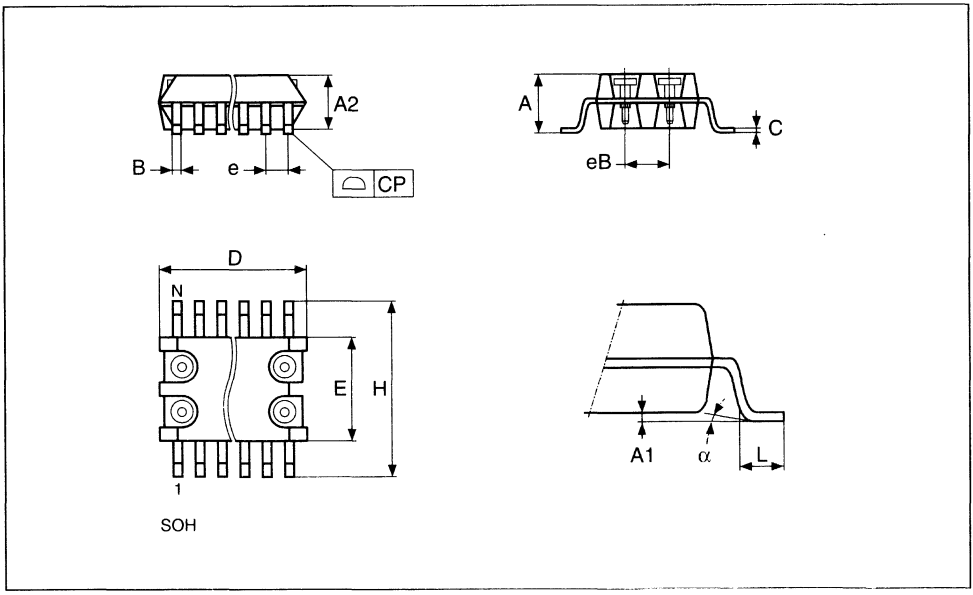
PCDIP

Drawing is not to scale

SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SOH28

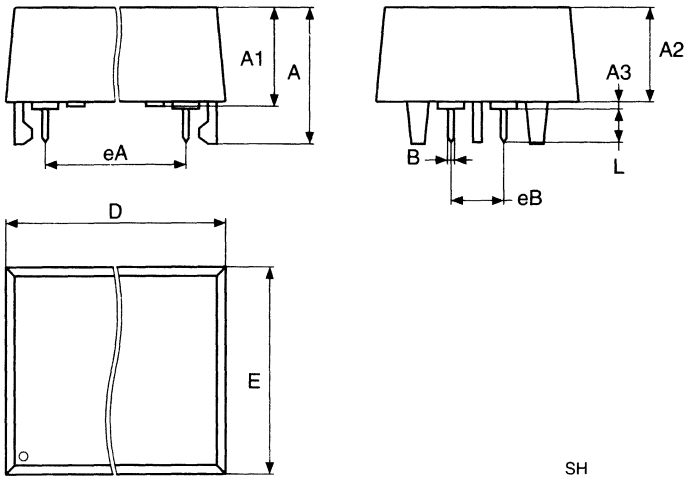


Drawing is not to scale

SH28 - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

SH28

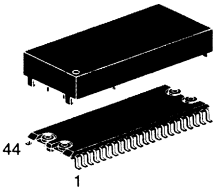


Drawing is not to scale

CMOS 32K x 8 TIMEKEEPER SRAM

PRODUCT PREVIEW

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT and BATTERY
- FREQUENCY TEST OUTPUT for REAL TIME CLOCK
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGE:
  - M48T36Y: 4.2V ≤ V_{PFD} ≤ 4.5V
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY and CRYSTAL
- SNAPHAT HOUSING (BATTERY and CRYSTAL) REPLACEABLE
- MICROPROCESSOR POWER-ON RESET
- PROGRAMMABLE ALARM OUTPUT ACTIVE in the BATTERY BACK-UP MODE
- BATTERY LOW WARNING



SOH44 (MH)
Battery SNAPHAT

Figure 1. Logic Diagram

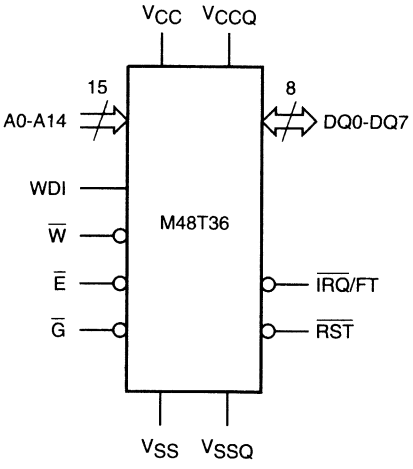


Table 1. Signal Names

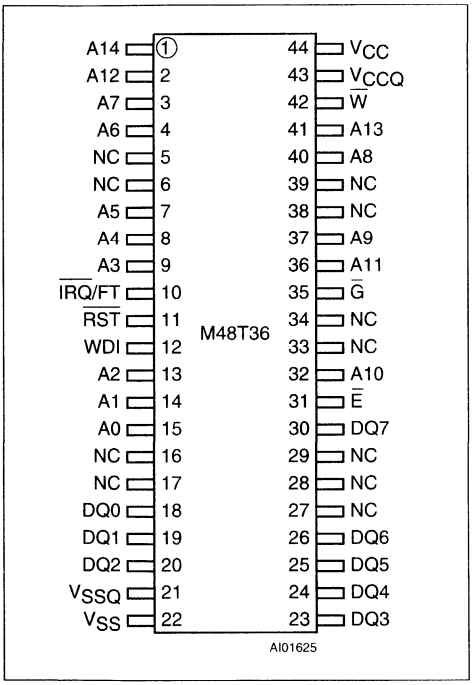
A0-A14	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{IRQ}$/FT	Interrupt / Frequency Test Output (Open Drain)
$\overline{RST}$	Power Fail Reset Output (Open Drain)
WDI	Watchdog Interrupt
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{CCQ}	Supply Voltage (DQ)
V_{SS}	Ground
V_{SSQ}	Ground (DQ)

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Figure 2A. DIP Pin Connections



Warning: NC = Not Connected

DESCRIPTION

The M48T36 TIMEKEEPER™ RAM is a 32K x 8 non-volatile static RAM and real time clock. The monolithic chip is available in a special package to provide a highly integrated battery backed-up memory and real time clock solution. The M48T36 is a non-volatile pin and function equivalent to any JEDEC standard 32K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The 44 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 44 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T44-BR12SH1".

As Figure 3 shows, the static memory array and the quartz controlled clock oscillator of the M48T36 are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 7FF9h-7FFFh. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically.

Figure 3. Block Diagram

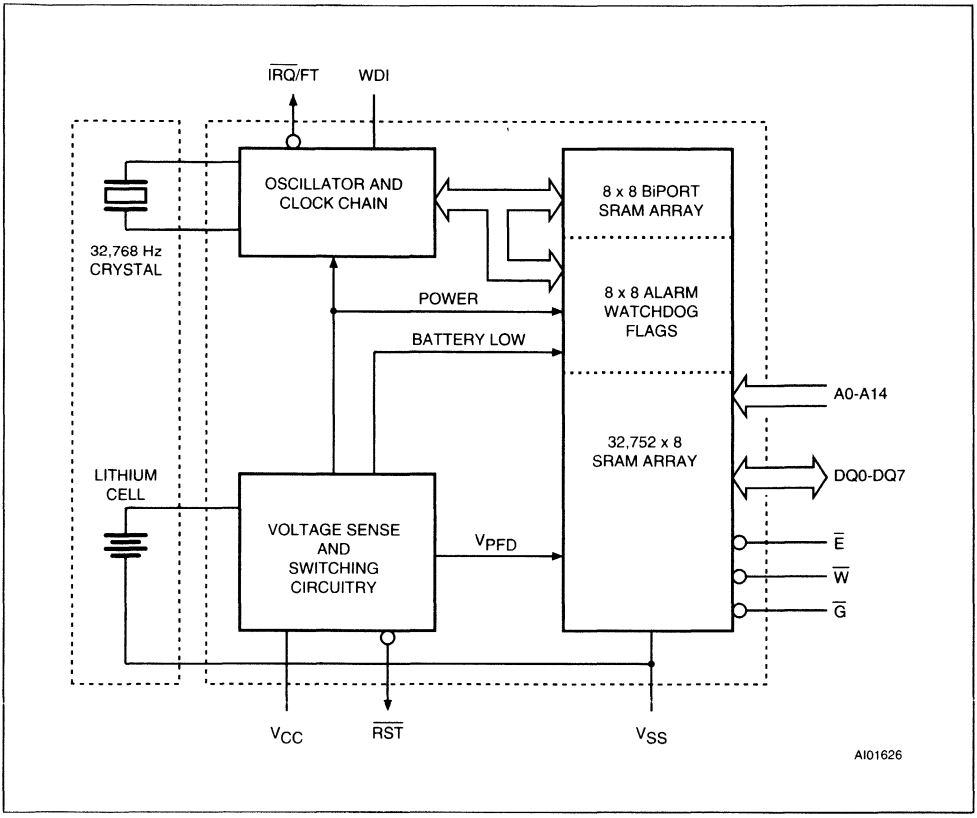


Table 3. Operating Modes (1)

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min) (2)	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	High Z	Battery Back-up Mode

Notes: 1. X = V_{IH} or V_{IL}
2. See Table 6 for details.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

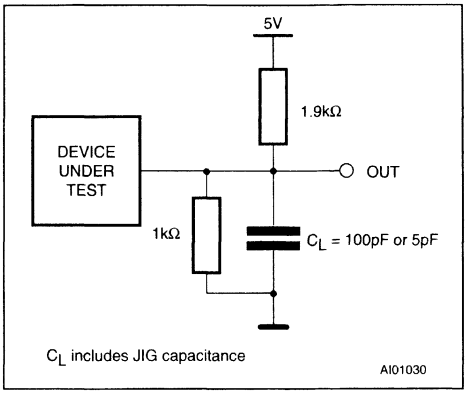


Table 4. Capacitance (1, 2) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} (3)	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} (1)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±5	µA
I_{CC}	Supply Current	Outputs open		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ = V_{CC} – 0.2V		3	mA
V_{IL} (2)	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
	Output Low Voltage ($\overline{IRQ}$/FT and $\overline{RST}$) (3)	I_{OL} = 10mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Notes: 1. Outputs Deselected.
2. Negative spikes of –1V allowed for up to 10ns once per Cycle.
3. The $\overline{IRQ}$/FT and $\overline{RST}$ pins are Open Drain.

Table 6. Power Down/Up Trip Points DC Characteristics (1) (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48T36Y)	4.2	4.35	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} (2)	Expected Data Retention Time	7			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	10		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	V_{PFD} (max) to $\overline{RST}$ High	40	200	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

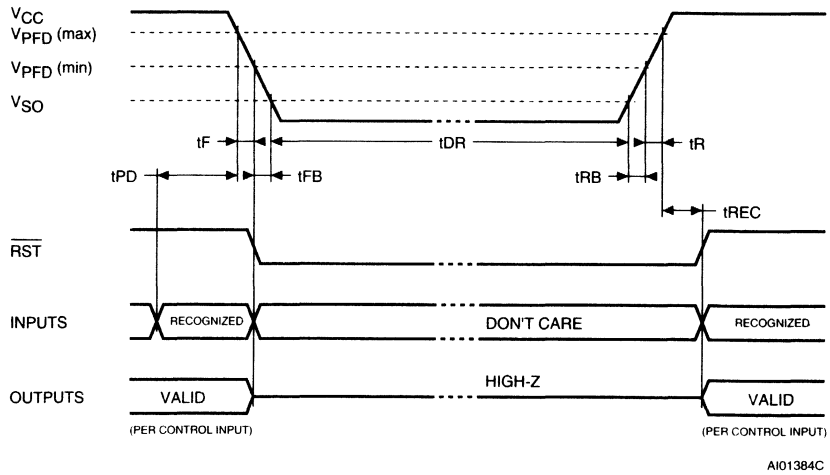
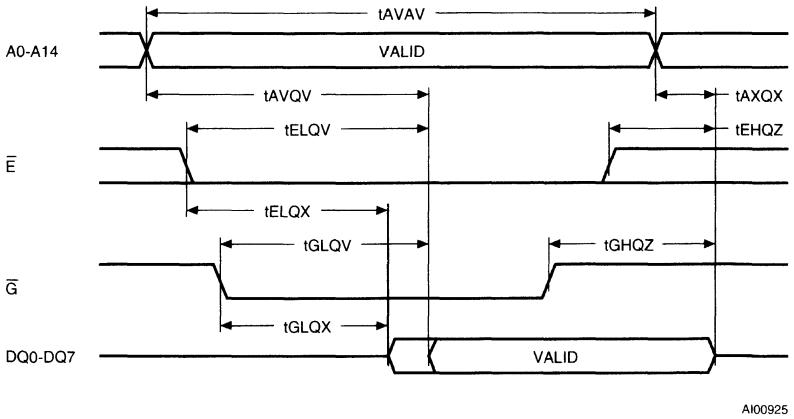


Table 8. Read Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	M48T36Y		Unit
		-70		
		Min	Max	
t_{AVAV}	Read Cycle Time	70		ns
t_{AVQV} (1)	Address Valid to Output Valid		70	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		70	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		35	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		25	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		ns

Notes: 1. C_L = 100pF (see Figure 4).
2. C_L = 5pF (see Figure 4).

Figure 6. Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High

Table 9. Write Mode AC Characteristics
(T_A = 0 to 70°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	M48T36Y		Unit
		-70		
		Min	Max	
t_{AVAV}	Write Cycle Time	70		ns
t_{AVWL}	Address Valid to Write Enable Low	0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		ns
t_{WLWH}	Write Enable Pulse Width	50		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	55		ns
t_{WHAX}	Write Enable High to Address Transition	0		ns
t_{EHAX}	Chip Enable High to Address Transition	0		ns
t_{DVWH}	Input Valid to Write Enable High	30		ns
t_{DVEH}	Input Valid to Chip Enable High	30		ns
t_{WHDX}	Write Enable High to Input Transition	5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		ns
t_{WLQZ} (1, 2)	Write Enable Low to Output Hi-Z		25	ns
t_{AVWH}	Address Valid to Write Enable High	60		ns
t_{AVE1H}	Address Valid to Chip Enable High	60		ns
t_{WHQX} (1, 2)	Write Enable High to Output Transition	5		ns

Notes: 1. C_L = 5pF (see Figure 4).
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

DESCRIPTION (cont'd)

Byte 7FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

Byte 7FF7h contains the watchdog timer setting. The watchdog timer detects an out-of-control microprocessor and provides a reset or interrupt to it. Byte 7FF2h-7FF5h are reserved for clock alarm programming. These bytes can be used to set the alarm. This will generate an active low signal on the $\overline{IRQ}$/FT pin when the alarm bytes match the date, hours, minutes and seconds of the clock.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ read/write memory cells. The M48T36 includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T36 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

READ MODE

The M48T36 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The unique address specified by the 15 Address Inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met,

Figure 7. Write Enable Controlled, Write AC Waveforms

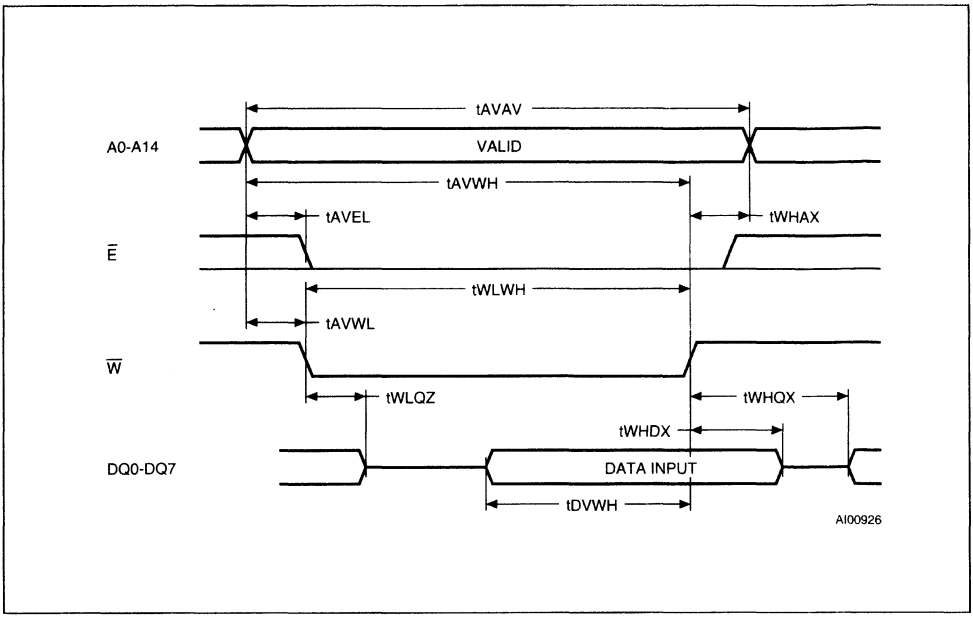
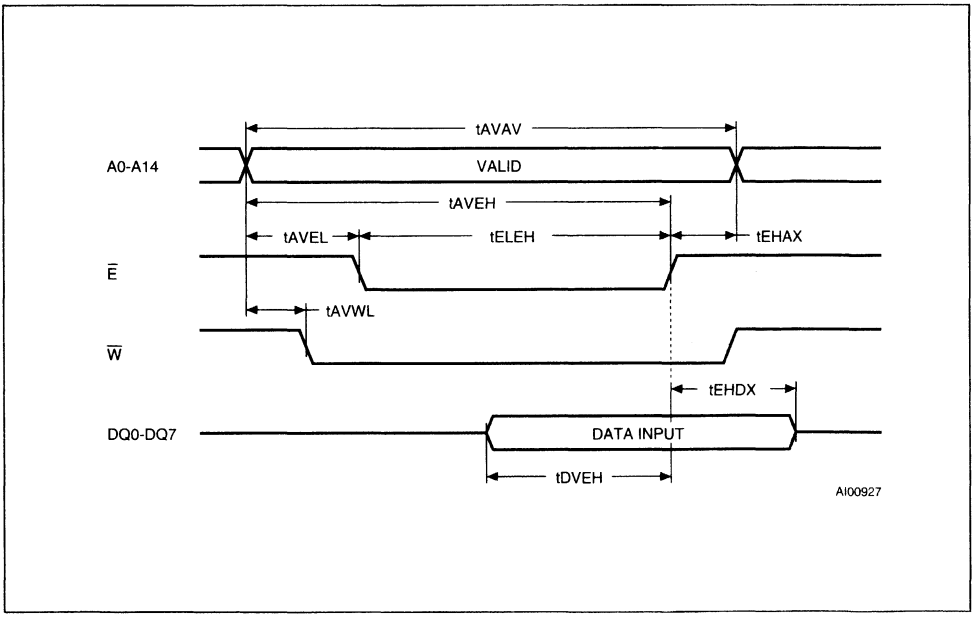


Figure 8. Chip Enable Controlled, Write AC Waveforms



READ MODE (cont'd)

valid data will be available after the latter of the Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48T36 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are low. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimumof t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$ a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48T36 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T36 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T36 for an accumulated period of at least 7 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Deselect continues for t_{REC} after V_{CC} reaches V_{PFD}(max).

POWER-ON RESET

The M48T36 continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ pulls low (open drain) and remains low on power-up for 40ms to 200ms after V_{CC} passes V_{PFD}. A 1kΩ resistor is recommended in order to control the rise time. The reset pulse remains active with V_{CC} at V_{SS}.

PROGRAMMABLE INTERRUPTS

The M48T36 has two programmable interrupts: an alarm and a watchdog. When an interrupt condition occurs, the M48T36 sets the appropriate flag bit in the flag register 7FF0h. The interrupt enable bits in 7FF6h and the WDS (Watchdog Steering) bit in 7FF7h allow the interrupt to activate the $\overline{IRQ}$/FT pin.

The interrupt flags and the $\overline{IRQ}$/FT output are cleared by a read to the flags register. An interrupt condition reset will not occur unless the addresses are stable at the flag location for at least 15ns while the device is in the read mode as shown in Figure 10.

The $\overline{IRQ}$/FT pin is an open drain output and requires a pull-up resistor. The pin remains in the high impedance state unless an interrupt occurs or the frequency test mode is enabled.

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

CLOCK OPERATIONS (cont'd)

Updating is halted when a '1' is written to the READ bit, D6 in the Control Register 7FF8h. As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0'.

Setting the Clock

Bit D7 of the Control Register 7FF8h is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 10). Resetting the WRITE bit to a '0' then transfers the values of all time registers 7FF9h-7FFFh to the actual TIMEKEEPER counters and allows normal operation to resume. After the WRITE bit is reset, the next clock update will occur in one second.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T36 is shipped from SGS-THOMSON with the STOP bit set to a '1'.

Table 10. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
7FFFh	10 Years				Year				Year	00-99
7FFEh	0	0	0	10 M.	Month				Month	01-12
7FFDh	0	0	10 Date		Date				Date	01-31
7FFCh	0	FT	0	0	0	Day			Day	01-07
7FFBh	0	0	10 Hours		Hours				Hour	00-23
7FFAh	0	10 Minutes			Minutes				Minutes	00-59
7FF9h	ST	10 Seconds			Seconds				Seconds	00-59
7FF8h	W	R	S	Calibration					Control	
7FF7h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
7FF6h	AFE	Y	ABE	Y	Y	Y	Y	Y	Interrupts	
7FF5h	RPT4	Y	Al. 10 Date		Alarm Date				Alarm Date	01-31
7FF4h	RPT3	Y	Al. 10 Hours		Alarm Hours				Alarm Hours	00-23
7FF3h	RPT2	Alarm 10 Minutes			Alarm Minutes				Alarm Minutes	00-59
7FF2h	RPT1	Alarm 10 Seconds			Alarm Seconds				Alarm Seconds	00-59
7FF1h	Y	Y	Y	Y	Y	Y	Y	Y	Unused	
7FF0h	WDF	AF	Z	BL	Z	Z	Z	Z	Flags	

Keys: **S** = SIGN Bit
FT = FREQUENCY TEST Bit
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to '0'
Y = '1' or '0'
Z = '0' and are Read only
AF = Alarm Flag
BL = Battery Low
WDS = Watchdog Steering Bit
BMB0–BMB4 = Watchdog Multiplier Bits
RB0–RB1 = Watchdog Resolution Bits
AFE = Alarm Flag Enable
ABE = Alarm in Battery Back-up Mode Enable
RPT1–RPT4 = Alarm Repeat Mode Bits
WDF = Watchdog Flag

When reset to a '0', the M48T36 oscillator starts within 1 second.

Calibrating the Clock

The M48T36 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. With the calibration bits properly set, the accuracy of each M48T36 improves to better than ±4 PPM at 25°C.

Of course the oscillation rate of any crystal changes with temperature. Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M48T36 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 9. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits (D4-D0) in the Control Register 7FF8h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

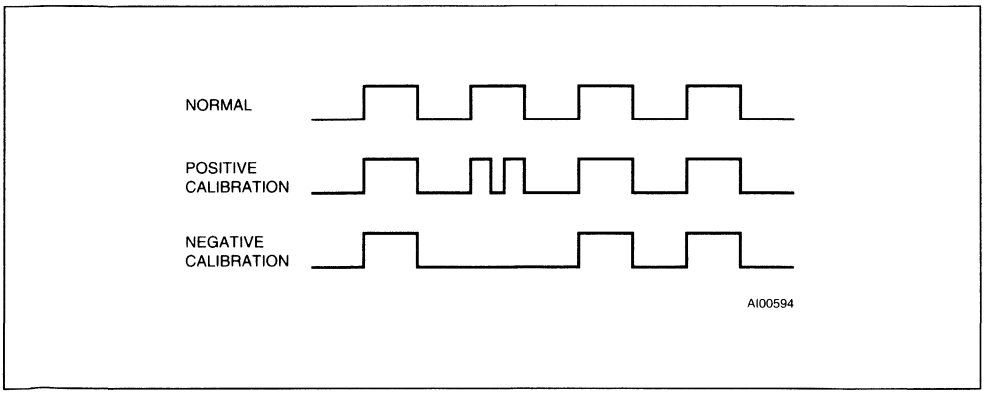
Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or -2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or - 5.35 seconds per month which corresponds to a total range of +5.5 or - 2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48T36 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{IRQ}$/FT pin. The pin will toggle at 512Hz when the Stop bit (D7 of 7FF9h) is '0', the FT bit (D6 of 7FFCh) is '1', the AFE bit (D7 of 7FF6h) is '0', and the Watchdog Steering bit (D7 of 7FF7h) is '1' or the Watchdog Register is reset (7FF7h = 0).

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a -10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

Figure 9. Clock Calibration



CLOCK OPERATIONS (cont'd)

The $\overline{IRQ}$/FT pin is an open drain output which requires a pull-up resistor for proper operation. A 500-10kΩ resistor is recommended in order to control the rise time. The FT bit is cleared on power-up.

SETTING ALARM CLOCK

Registers 7FF5h-7FF2h contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific day of the month or repeat every day, hour, minute, or second. It can also be programmed to go off while the M48T36 is in the battery back-up mode of operation to serve as a system wake-up call.

RPT1-RPT4 put the alarm in the repeat mode of operation. Table 11 shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

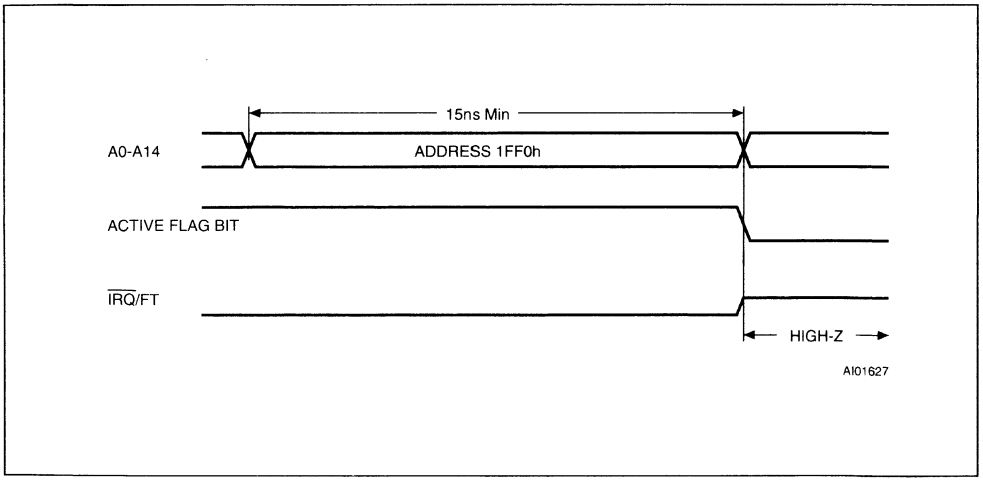
When the clock information matches the alarm clock settings based on the match criteria defined by RPT1-RPT4, AF (Alarm Flag) is set. If AFE (Alarm Flag Enable) is also set, the alarm condition activates the $\overline{IRQ}$/FT pin. The alarm flag and the $\overline{IRQ}$/FT output are cleared by a read to the Flags register as shown in Figure 10.

The $\overline{IRQ}$/FT pin can also be activated in the battery back-up mode. The $\overline{IRQ}$/FT will go low if an alarm occurs and both ABE (Alarm in Battery Back-up Mode Enable) and AFE are set. The ABE and AFE bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the Flag Register at system boot-up to determine if an alarm was generated while the M48T36 was in the deselect mode during power-up. Figure 11 illustrates the back-up mode alarm timing.

Table 11. Alarm Repeat Mode

RPT4	RPT3	RPT2	RPT1	Alarm Activated
1	1	1	1	Once per Second
1	1	1	0	Once per Minute
1	1	0	0	Once per Hour
1	0	0	0	Once per Day
0	0	0	0	Once per Month

Figure 10. Interrupt Reset Waveforms



WATCHDOG TIMER

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the eight bit Watchdog Register, address 7FF7h. The five bits (BMB4-BMB0) store a binary multiplier and the two lower order bits (RB1-RB0) select the resolution, where 00=1/16 second, 01=1/4 second, 10=1 second, and 11=4 seconds. The amount of time-out is then determined to be the multiplication of the five bit multiplier value with the resolution. (For example: writing 00001110 in the Watchdog Register = 3 x 1 or 3 seconds). If the processor does not reset the timer within the specified period, the M48T36 sets the WDF (Watchdog Flag) and generates a watchdog interrupt or a microprocessor reset.

The most significant bit of the Watchdog Register is the Watchdog Steering Bit. When set to a '0', the watchdog will activate the $\overline{IRQ}$/FT pin when timed-out. When WDS is set to a '1', the watchdog will output a negative pulse on the $\overline{RST}$ pin for a duration of 40ms to 200ms. The Watchdog register and the FT bit will reset to a '0' at the end of a watchdog time-out when the WDS bit is set to a '1'.

The watchdog timer resets when the microprocessor performs a read of the Watchdog Register. The time-out period then starts over. The watchdog timer is disabled by writing a value of 00000000 to the eight bits in the Watchdog Register. The watchdog function is automatically disabled upon power-up and the Watchdog Register is cleared. If the watchdog function is set to output to the $\overline{IRQ}$/FT pin and the frequency test function is activated, the watchdog function prevails and the frequency test function is denied. The WDI pin contains a pull-up resistor which is greater than 100kΩ, and therefore can be left unconnected if not used.

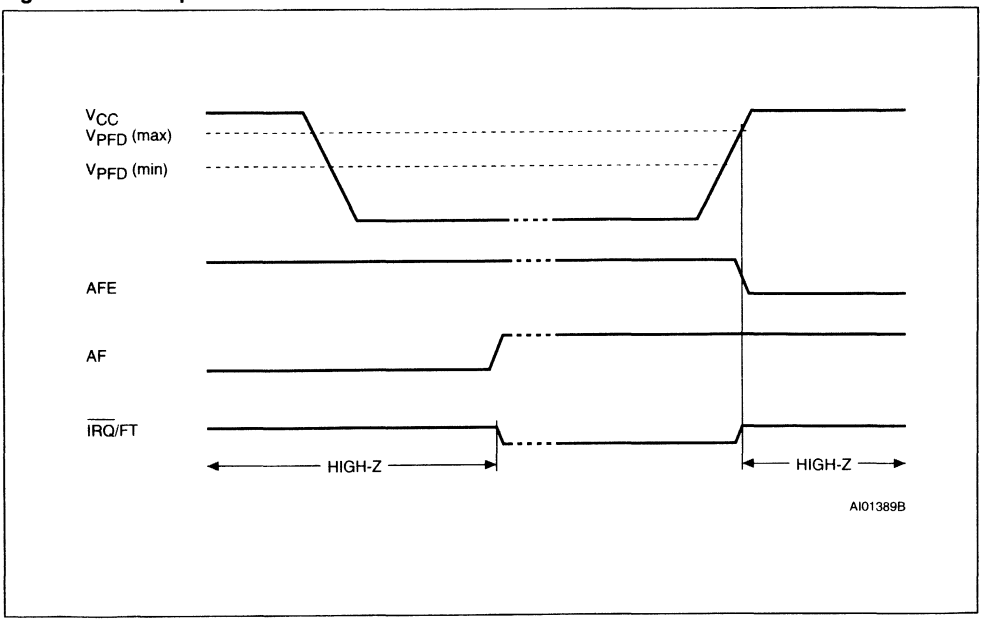
BATTERY LOW WARNING

The M48T36 checks it's battery voltage on power-up. The BL (Battery Low) bit D4 of 7FF0h will be set on power-up if the battery voltage is less than 2.5V (typical).

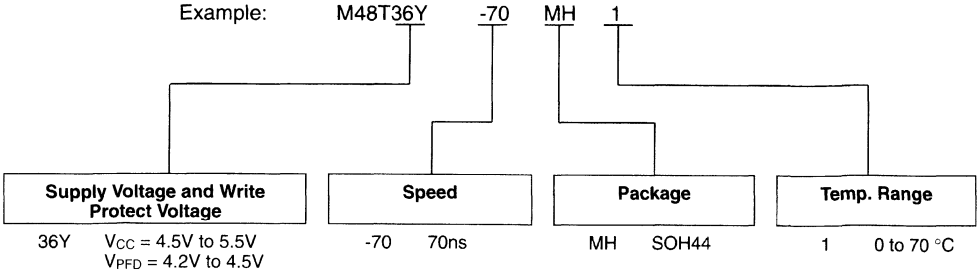
POWER-ON DEFAULTS

Upon application of power to the device, the following register bits are set to a '0' state: WDS = 0; BMB0-BMB4 = 0; RB0-RB1 = 0; AFE = 0; ABE = 0.

Figure 11. Back-up Mode Alarm Waveforms



ORDERING INFORMATION SCHEME



The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 44 lead SO, the battery package (i.e. SNAPHAT) part number is "M4T44-BR12SH1".

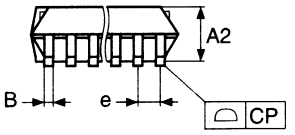
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

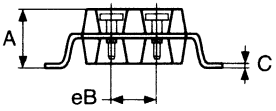
For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

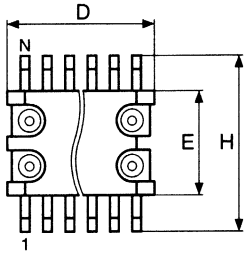
SOH44 - 44 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D	–	–	–	–	–	–
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N		44			44	
CP			0.10			0.004

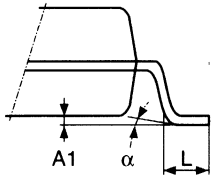
SOH44







SOH

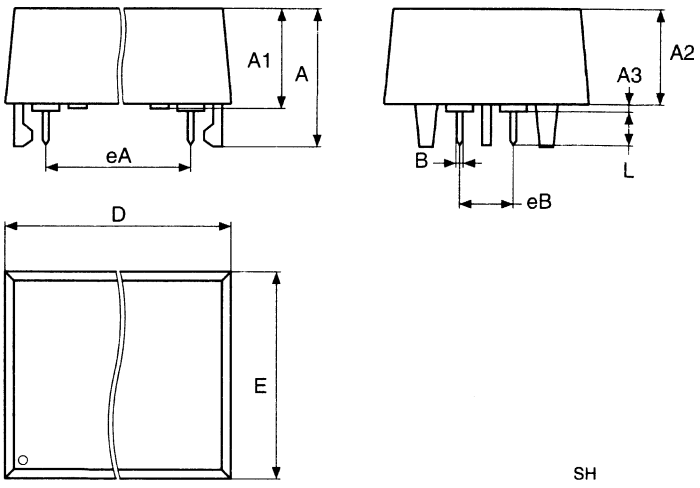


Drawing is not to scale

SH44 - SNAPHAT Housing for 44 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D	–	–	–	–	–	–
E		14.22	14.99		0.560	0.590
eA	–	–	–	–	–	–
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

SH44



Drawing is not to scale

DEDICATED NVRAM

CMOS 64 x 8 SERIAL ACCESS TIMEKEEPER SRAM

- COUNTERS for SECONDS, MINUTES, HOURS, DAY, DATE, MONTH and YEARS
- SOFTWARE CLOCK CALIBRATION
- AUTOMATIC POWER FAIL DETECT and SWITCH CIRCUITRY
- I^2C BUS COMPATIBLE
- 56 BYTES of GENERAL PURPOSE RAM
- ULTRA-LOW BATTERY SUPPLY CURRENT of 500nA
- AVAILABLE with an OPERATING TEMPERATURE of –40 to 85°C
- AUTOMATIC LEAP YEAR COMPENSATION

PSDIP8 (N)
0.4mm Frame

SO8 (S)
0.15mm Frame

DESCRIPTION

The MK41T56 TIMEKEEPER™ RAM is a low power 512 bit static CMOS RAM organized as 64 words by 8 bits. A built-in 32.768 kHz oscillator (external crystal controlled) and the first 8 bytes of the RAM are used for the clock/calendar function and are configured in BCD format. Addresses and data are transferred serially via a two-line bi-directional bus. The built-in address register is incremented automatically after each write or read data byte. The MK41T56 clock has a built-in power sense circuit which detects power failures and automatically switches to the battery supply during power failures. The energy needed to sustain the RAM and clock operations can be supplied from a small lithium button cell.

Table 1. Signal Names

OSCI	Oscillator Input
OCSO	Oscillator Output
FT/OUT	Frequency Test / Output Driver
SDA	Serial Data Address Input / Output
SCL	Serial Clock
V_{BAT}	Battery Supply Voltage
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

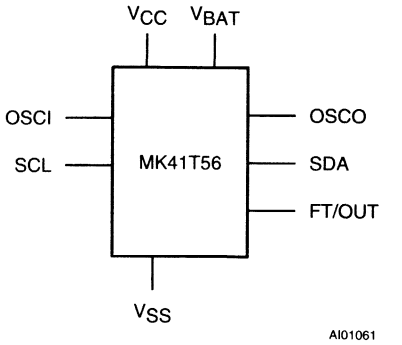


Figure 2A. DIP Pin Connections

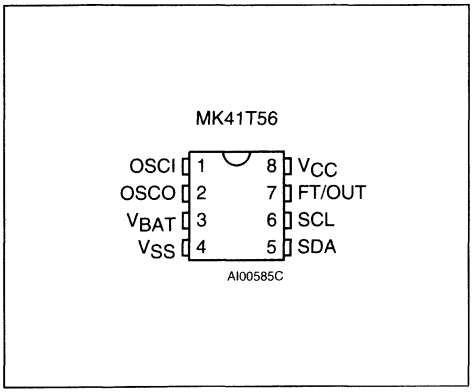


Figure 2B. SO Pin Connections

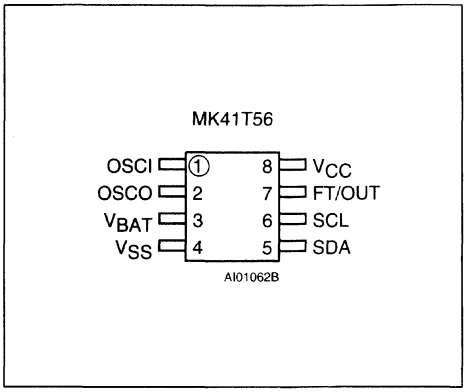


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–55 to 125	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	0.25	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

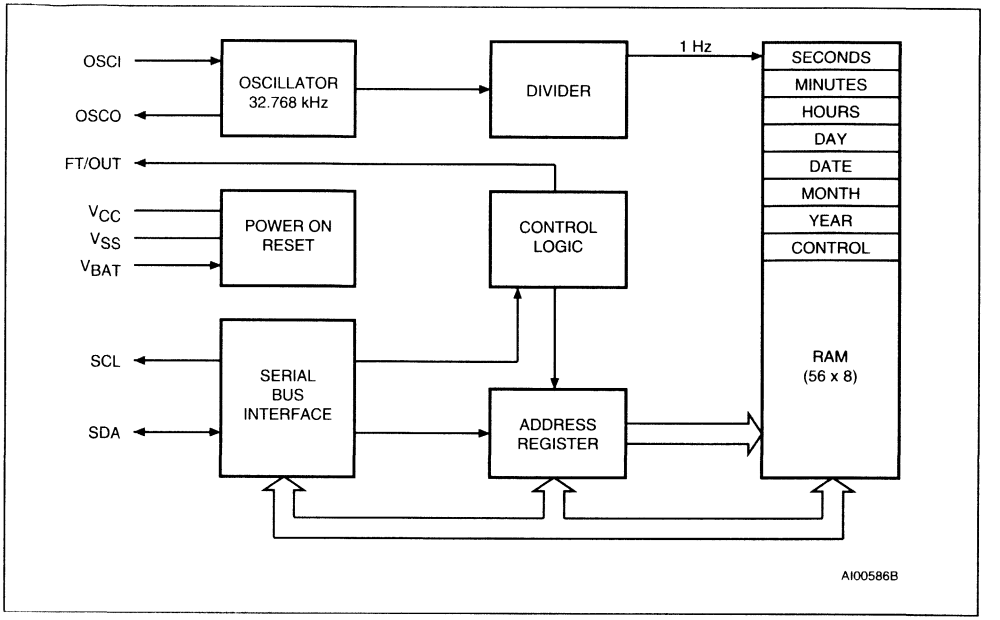
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
0	ST	10 Seconds			Seconds				Seconds	00-59
1	X	10 Minutes			Minutes				Minutes	00-59
2	X	X	10 Hours		Hours				Hour	00-23
3	X	X	X	X	X	Day			Day	01-07
4	X	X	10 Date		Date				Date	01-31
5	X	X	X	10 M.	Month				Month	01-12
6	10 Years				Years				Year	00-99
7	OUT	FT	S	Calibration					Control	

Keys: **S** = SIGN Bit; **FT** = FREQUENCY TEST Bit; **ST** = STOP Bit; **OUT** = Output level; **X** = Don't care.

Figure 3. Block Diagram



DESCRIPTION (cont'd)

Typical data retention time is in excess of 10 years with a 39 mA/h 3V lithium cell. The MK41T56 clock is supplied in 8 Pin Plastic Dual-in-Line and 8 pin Plastic Small Outline packages.

OPERATION

The MK41T56 clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct address (D0). The 64 bytes contained in the device can then be accessed sequentially in the following order:

1. Seconds Register
2. Minutes Register
3. Hours Register
4. Day Register
5. Date Register
6. Month Register
7. Years Register
8. Control Register

9 to 64. RAM

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

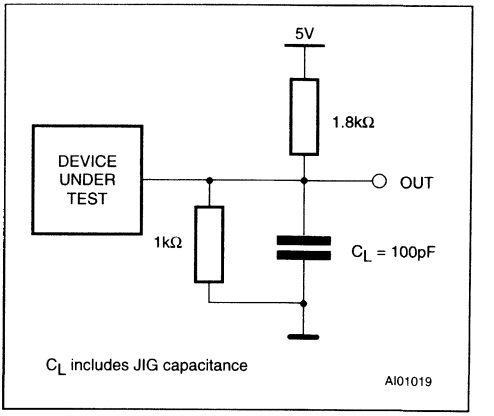


Table 4. Capacitance [1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (SCL)		7	pF
C_{OUT} [2]	Output Capacitance (SDA, FT/OUT)		10	pF

Notes: 1. Effective capacitance calculated from the equation C = IΔt/ΔV with ΔV = 3V and power supply at 5V.
2. Outputs deselected.

Table 5. DC Characteristics (T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}			±10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}			±10	µA
I_{CC1}	Supply Current	SCL/SDA = V_{CC}–0.3V			1	mA
I_{CC2}	Supply Current (Standby)				1	mA
V_{IL}	Input Low Voltage		–0.3		1.5	V
V_{IH}	Input High Voltage		3		V_{CC} + 0.8	V
V_{OL}	Output Low Voltage	I_{OL} = 5mA, V_{CC} = 4.5V			0.4	V
V_{BAT} [1]	Battery Supply Voltage		2.6	3	3.5	V
I_{BAT}	Battery Supply Current	T_A = 25°C, V_{CC} = 0V, Oscillator ON, V_{BAT} = 3V		450	500	nA

Note: SGS-THOMSON recommends the RAYOVAC BR1225 or equivalent as the battery supply.

Table 6. Power Down/Up Trip Points DC Characteristics[1] (T_A = 0 to 70°C or –40 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage	1.2 V_{BAT}	1.25 V_{BAT}	1.285 V_{BAT}	V
V_{SO}	Battery Back-up Switchover Voltage		V_{BAT}		V

Note: 1. All voltages referenced to V_{SS}.

Table 7. Crystal Electrical Characteristics (Externally Supplied)

Symbol	Parameter	Min	Typ	Max	Unit
f_O	Resonant Frequency		32.768		kHz
R_S	Series Resistance			35	kΩ
C_L	Load Capacitance		12.5		pF

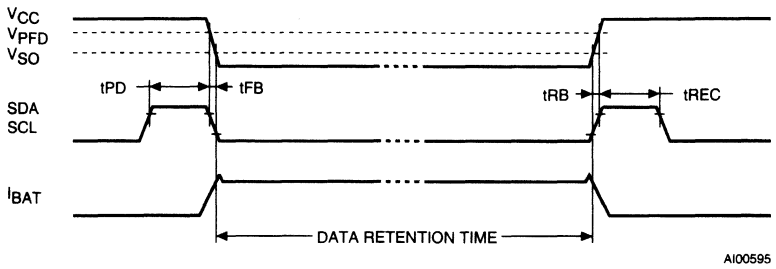
Notes: Load capacitors are internally supplied with the MK41T56. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

SGS-THOMSON recommends the ECS-.327-12.5-8SP-2 quartz crystal for industrial temperature operations. ESC Inc. can be contacted at 800-237-1041 or 913-782-7787 for further information on this crystal type.

Table 8. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C or –40 to 85°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	SCL and SDA at V_{IH} before Power Down	0		ns
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	300		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	100		µs
t_{REC}	SCL and SDA at V_{IH} after Power Up	200		µs

Figure 5. Power Down/Up Mode AC Waveforms



OPERATION (cont'd)

The MK41T56 clock continually monitors V_{CC} for an out of tolerance condition. Should V_{CC} fall below V_{PFD} the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out of tolerance system. When V_{CC} falls below V_{BAT} the device automatically switches over to the battery and powers down into an ultra low current mode of operation to conserve battery life. Upon power up the device switches from battery to V_{CC} at V_{BAT} and recognizes inputs when V_{CC} goes above V_{PFD} volts.

2-WIRE BUS CHARACTERISTICS

This bus is intended for communication between different ICs. It consists of two lines: one bi-directional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is High. Changes in the data line while the clock line is High will be interpreted as control signals.

Table 9. AC Characteristics (T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Min	Max	Unit
f_{SCL}	SCL Clock Frequency	0	100	kHz
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4		µs
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{HD:STA}$	START Condition Hold Time (after this period the first clock pulse is generated)	4		µs
$t_{SU:STA}$	START Condition Setup Time (only relevant for a repeated start condition)	4.7		µs
$t_{SU:DAT}$ (1)	Data Setup Time	250		ns
$t_{HD:DAT}$	Data Hold Time	0		µs
$t_{SU:STO}$	STOP Condition Setup Time	4.7		µs
t_{BUF}	Time the bus must be free before a new transmission can start	4.7		µs
t_I	Noise suppresion time constant at SCL and SDA input	0.25	1	µs

Note: 1. Transmitter must internally provide a hold time to bridge the undefined region (300ns max.) of the falling edge of SCL.

2-WIRE BUS CHARACTERISTICS (cont'd)

Accordingly, the following bus conditions have been defined:

Bus not busy. Both data and clock lines remain High.

Start data transfer. A change in the state of the data line, from High to Low, while the clock is High, defines the START condition.

Stop data transfer. A change in the state of the data line, from Low to High, while the clock is High, defines the STOP condition.

Data valid. The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the High period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a nineth bit.

Within the bus specifications a low speed mode (2kHz clock rate) and a high speed mode (100kHz clock rate) are defined. The MK41T56 clock works in both modes. By definition a device that gives out a message is called "transmitter", the receiving device that gets the message is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves".

Acknowledge. Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the High period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal

Figure 6. Serial Bus Data Transfer Sequence

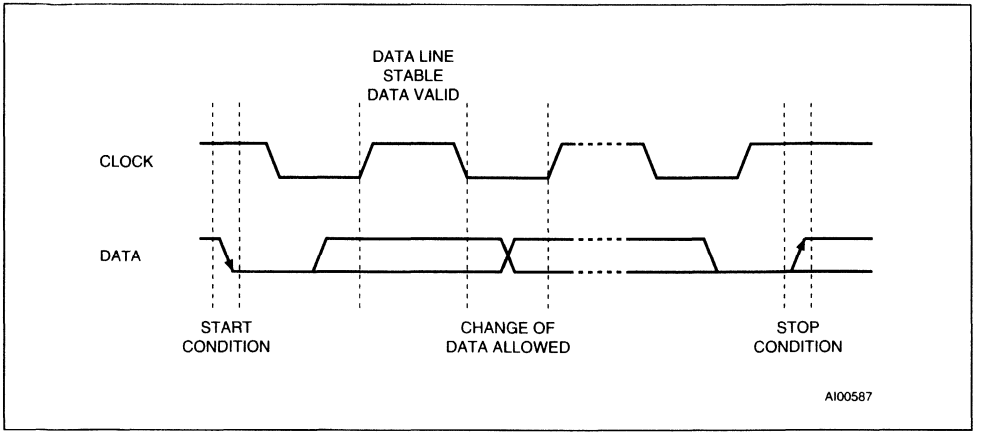


Figure 7. Acknowledgement Sequence

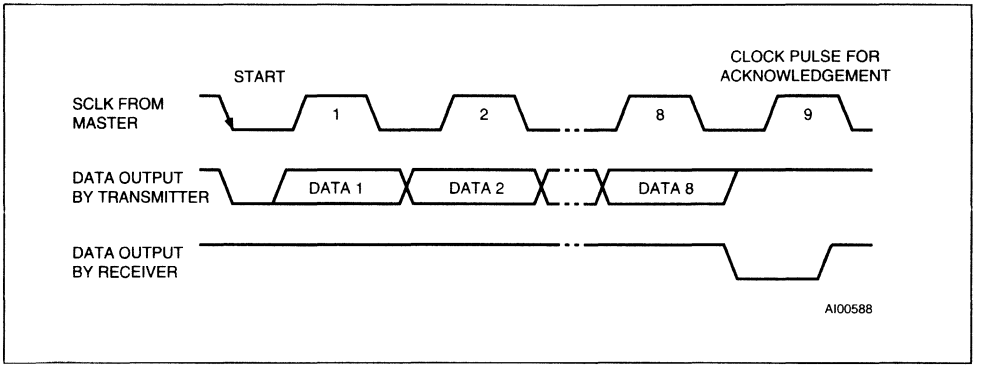
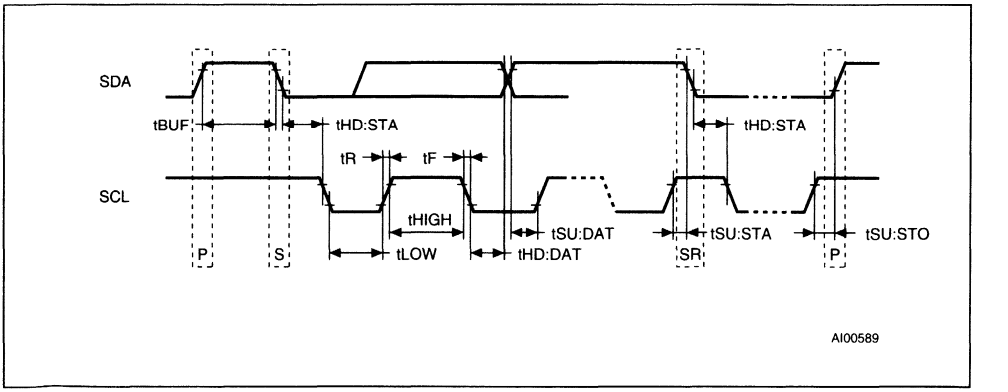


Figure 8. Bus Timing Requirements Sequence



2-WIRE BUS CHARACTERISTICS (cont'd)

an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line High to enable the master to generate the STOP condition.

WRITE MODE

In this mode the master transmitter transmits to the MK41T56 slave receiver. Bus protocol is shown in Figure 10. Following the START condition and slave address, a logic '0' ($R/\overline{W}$ = 0) is placed on the bus and indicates to the addressed device that word address A_n will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The MK41T56 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte, see Figure 9.

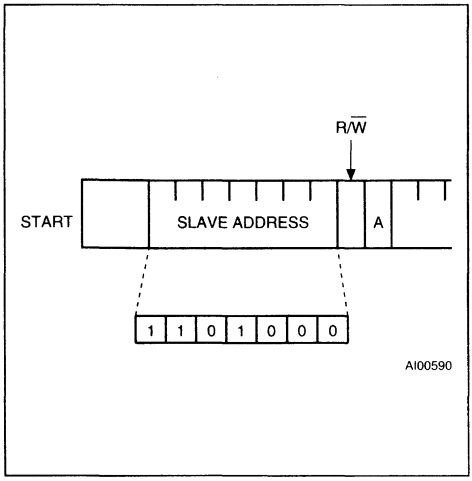
READ MODE

In this mode the master reads the MK41T56 slave after setting the slave address, see Figure 11. Following the write mode control bit ($R/\overline{W}$ = 0) and the acknowledge bit, the word address A_n is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit ($R/\overline{W}$ = 1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The MK41T56 slave transmitter will now place the data byte at address An + 1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to An + 2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented whereby the master reads the MK41T56 slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer, see Figure 12.

Figure 9. Slave Address Location



CLOCK CALIBRATION

The MK41T56 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. A typical MK41T56 is accurate within ± 1 minute per month at 25°C without calibration. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature.

Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The MK41T56 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in Figure 13. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minutes cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minutes cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is + 4.068 or –2.034 PPM of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz,

Figure 10. Write Mode Sequence

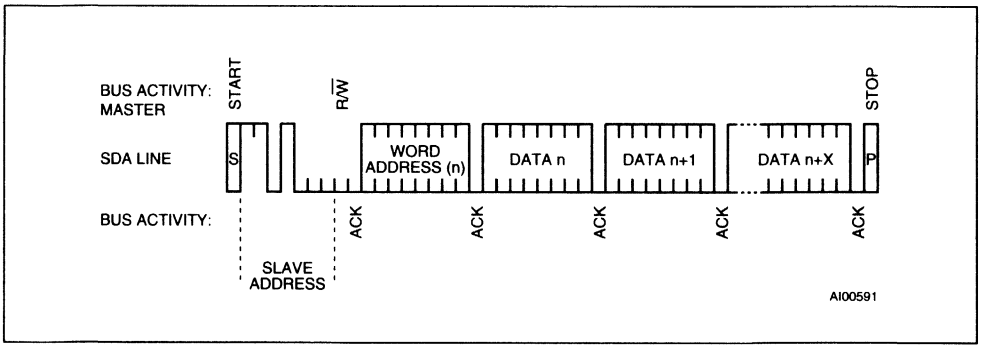


Figure 11. Read Mode Sequence

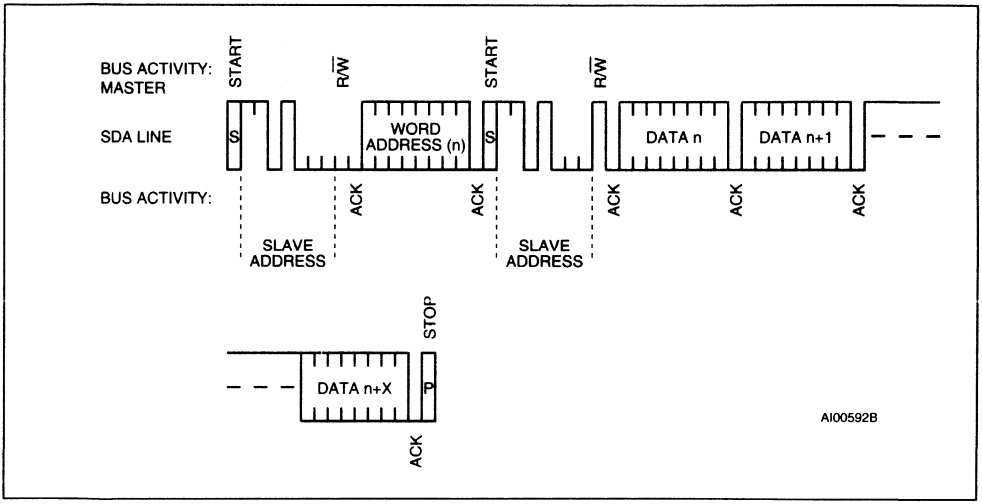
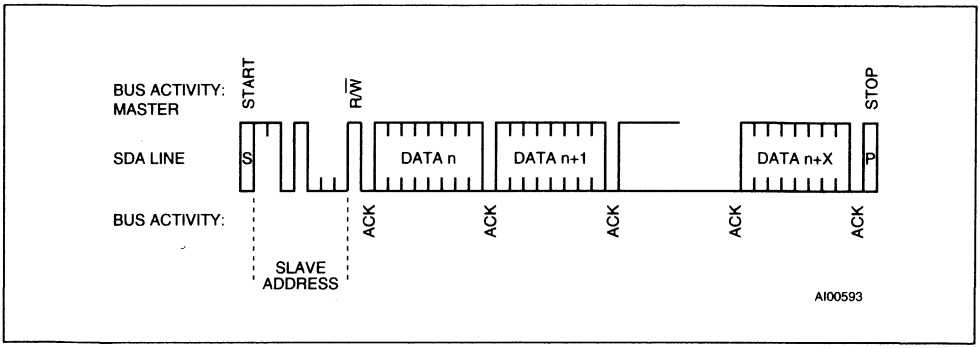


Figure 12. Alternate Read Mode Sequence



CLOCK CALIBRATION (cont'd)

each of the 31 increments in the Calibration byte would represent 10.7 seconds per month.

Two methods are available for ascertaining how much calibration a given MK41T56 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accessed the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Control Register, is set to a '1', and the oscillator is running at 32,768 Hz, the FT/OUT pin of the device will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature.

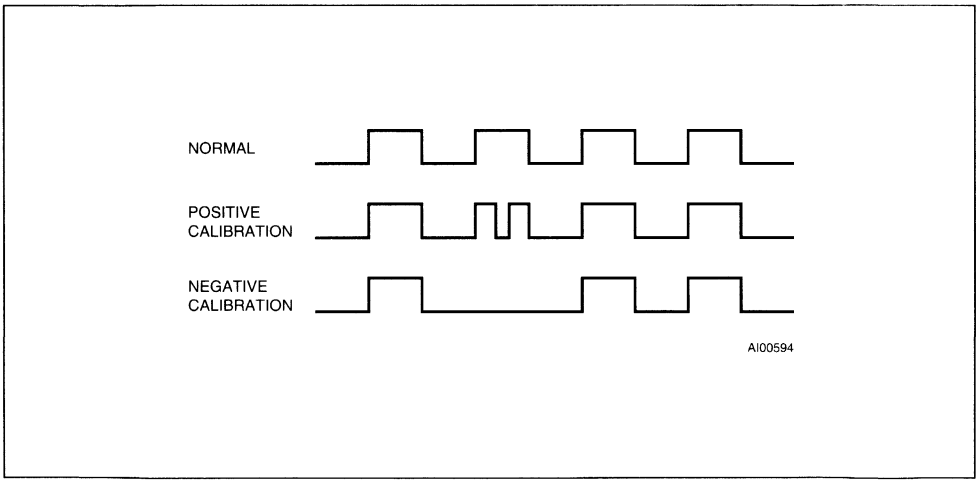
For example, a reading of 512.01024 Hz would indicate a +20 PPM oscillator frequency error, requiring a –10(001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

OUTPUT DRIVER PIN

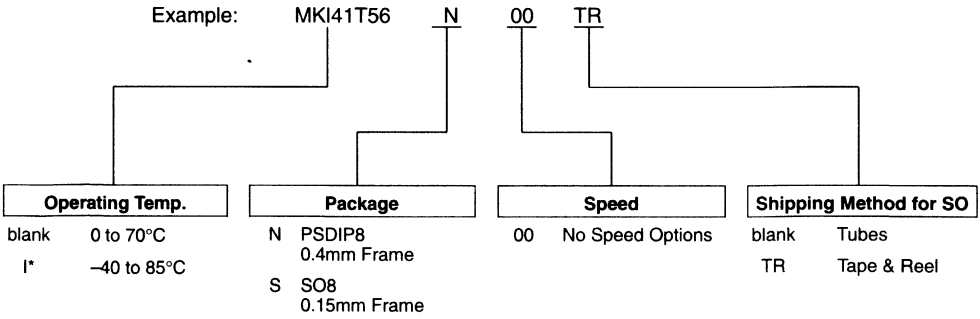
When the FT bit is not set the FT/OUT pin becomes an output driver that reflects the contents of D7 of the control register. In other words when D6 of location 7 is a zero and D7 of location 7 is a zero and then the FT/OUT pin will be driven low.

Note: The FT/OUT pin is open drain which requires an external pull-up resistor.

Figure 13. Divide by 128 Stage



ORDERING INFORMATION SCHEME



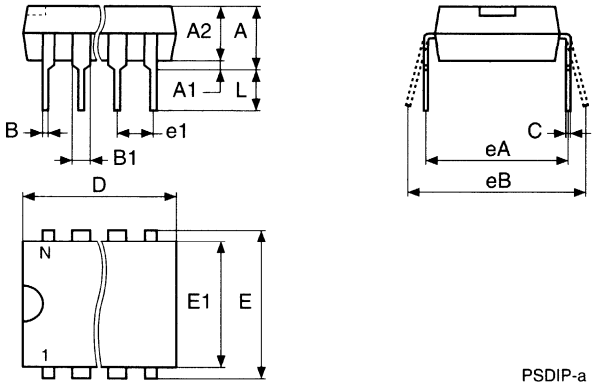
Note: I* Available in the SO package only.

For a list of available options refer to the current Memory Shortform catalogue.
For further information or any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.4mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.80			0.189
A1		0.70	–		0.028	–
A2		3.10	3.60		0.122	0.142
B		0.38	0.58		0.015	0.023
B1		1.15	1.65		0.045	0.065
C		0.38	0.52		0.015	0.020
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.30	7.10		0.248	0.280
e1	2.54	–	–	0.100	–	–
eA		8.40	–		0.331	–
eB			9.20			0.362
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



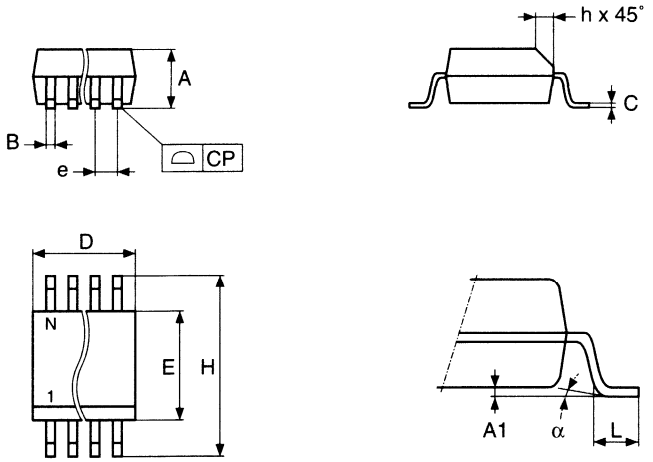
PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004

SO8



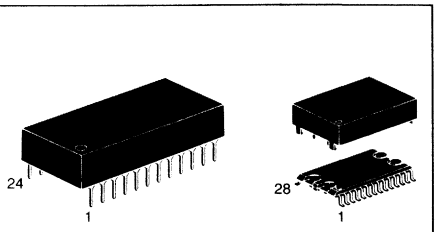
SO-a

Drawing is not to scale

5 VOLT PC REAL TIME CLOCK

PRODUCT PREVIEW

- DROP-IN REPLACEMENT for PC-AT COMPUTER CLOCK/CALENDAR
- COUNTS SECONDS, MINUTES, HOURS, DAYS, DAY of the WEEK, DATE, MONTH and YEAR with LEAP YEAR COMPENSATION
- INTERFACED WITH SOFTWARE AS 128 RAM LOCATIONS:
  - 14 Bytes of Clock and Control Registers
  - 114 Bytes of General Purpose RAM
- BUS COMPATIBLE INTERRUPT SIGNAL (IRQ)
- SELECTABLE BUS TIMING
- THREE INTERRUPTS are SEPARATELY SOFTWARE-MASKABLE and TESTABLE
  - Time-of-Day Alarm (Once/Second to Once/Day)
  - Periodic Rates from 122µs to 500ms
  - End-of-Clock Update Cycle
- PROGRAMMABLE SQUARE WAVE OUTPUT
- SELF CONTAINED BATTERY and CRYSTAL in the CAPHAT DIP PACKAGE
- SMALL OUTLINE PACKAGE PROVIDES DIRECT CONNECTION for a SNAPHAT HOUSING CONTAINING the BATTERY and CRYSTAL
- COMPATIBLE with bq3285/7 and DS12887



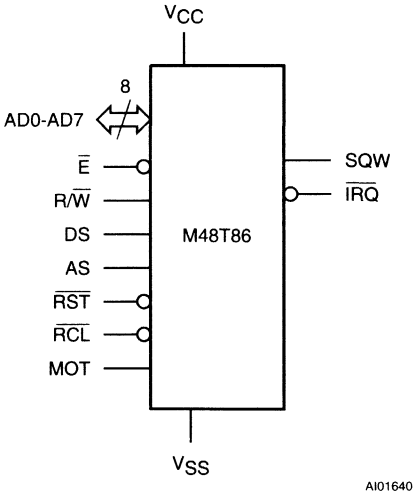
PCDIP24 (PC)
Battery CAPHAT

SOH28 (MH)
Battery SNAPHAT

Table 1. Signal Names

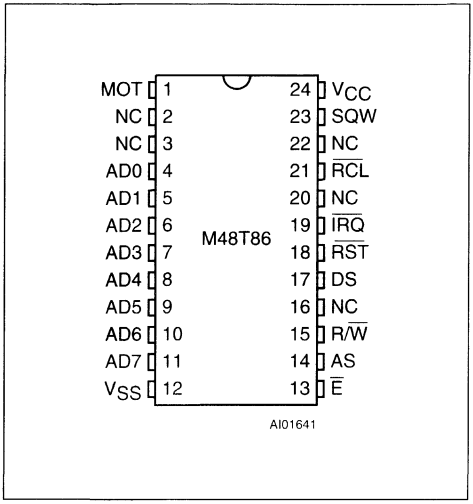
AD0-AD7	Multiplexed Address/Data Bus
$\overline{E}$	Chip Enable Input
R/$\overline{W}$	Write Enable Input
DS	Data Strobe Input
AS	Address Strobe Input
$\overline{RST}$	Reset Input
$\overline{RCL}$	RAM Clear Input
MOT	Bus Type Select Input
SQW	Square Wave Output
$\overline{IRQ}$	Interrupt Request Output
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



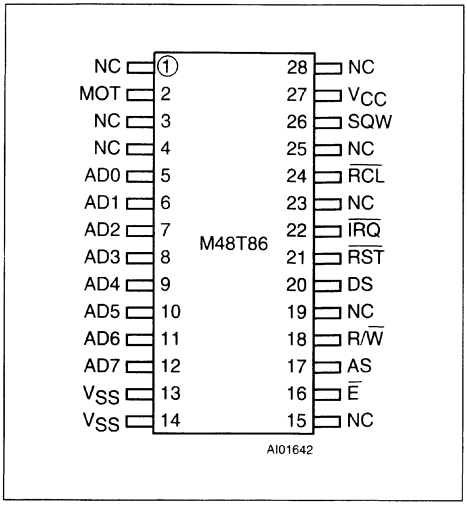
This is advance information on a new product now in development. Details are subject to change without notice.

Figure 2A. DIP Pin Connections



Warning: NC = Not Connected.

Figure 2B. SO Pin Connections



Warning: NC = Not Connected.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7.0	V
V_{CC}	Supply Voltage	–0.3 to 7.0	V
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

DESCRIPTION

The M48T86 is an industry standard real time clock (RTC). The M48T86 is composed of a lithium energy source, quartz crystal, write-protection circuitry, and a 128 byte RAM array. This provides the user with a complete subsystem packaged in either a 28-pin DIP CAPHAT or SNAPHAT SO. Functions available to the user include a non-volatile time-of-day clock, alarm interrupts, a one-hundred-year clock with programmable interrupts, square wave output, and 128 bytes of non-volatile static RAM.

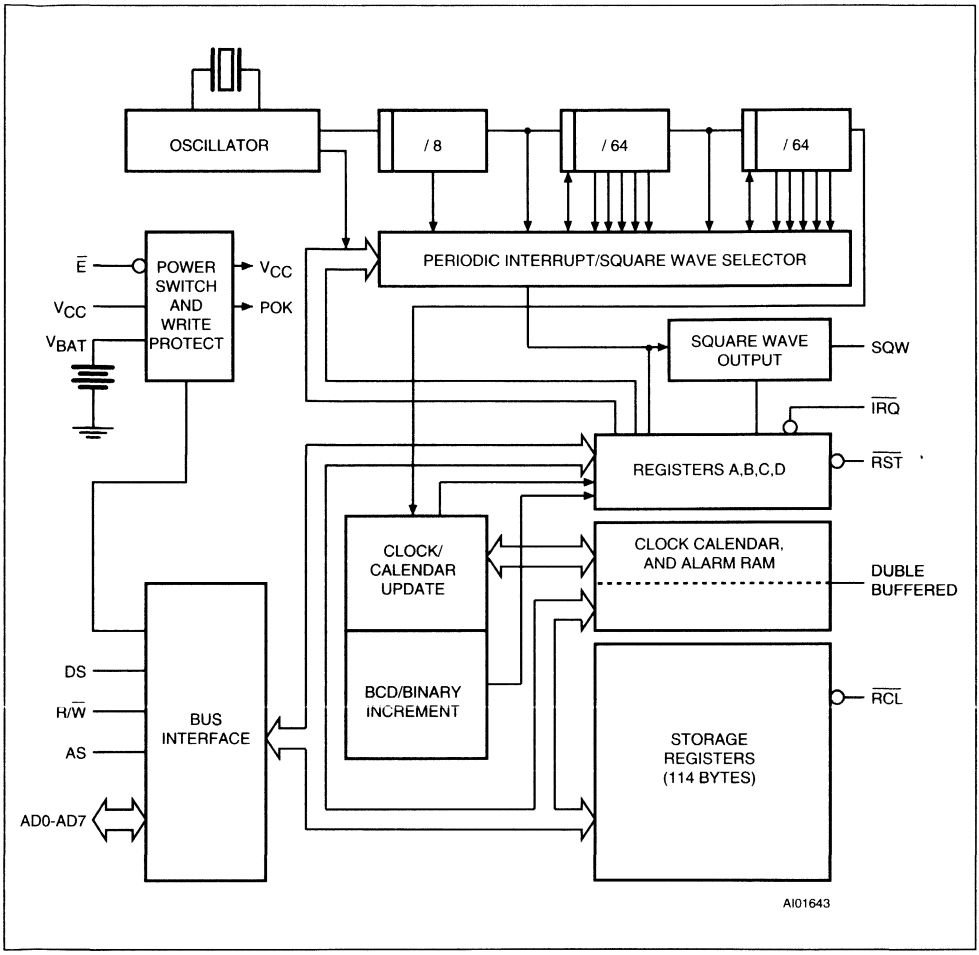
The 24 pin 600mil DIP CAPHAT™ houses the M48T86 silicon with a quartz crystal and a long life lithium button cell in a single package.

The 28 pin 330mil SO provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT™ housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SO package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form.

Figure 3. Block Diagram



For the 28 lead SO, the battery package part number is "M4T28-BR12SH1".

Automatic deselection of the device provides insurance that data integrity is not compromised should V_{CC} fall below specified (V_{PFD}) levels. The automatic deselection of the device remains in effect upon power up for a period of 200ms (max) after V_{CC} rises above V_{PFD}, provided that the Real Time Clock is running and the count down chain is not reset. This allows sufficient time for V_{CC} to stabilize and gives the system clock a wake up period so that a valid system reset can be established.

The block diagram in Figure 3 shows the pin connections and the major internal functions of the M48T86.

SIGNAL DESCRIPTION

V_{CC}, V_{SS}. DC power is provided to the device on these pins. The M48T86 utilizes a 5V V_{CC}.

SQW (Square Wave Output). During normal operation (i.e. valid V_{CC}), the SQW pin can output a signal from one of 13 taps. The frequency of the SQW pin can be changed by programming Regis-

SIGNAL DESCRIPTION (cont'd)

ters A as shown in Table 9. The SQW signal can be turned on and off using the SQWE bit (Register B; bit 3). The SQW signal is not available when V_{CC} is less than V_{PFD}.

AD0-AD7 (Multiplexed Bi-Directional Address/Data Bus). The M48T86 provides a multiplexed bus in which address and and information share the same signal path. The bus cycle consists of two stages; first the address is latched, followed by the data. Address/Data multiplexing does not slow the access time of the M48T86 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS, at which time the M48T86 latches the address present on AD0-AD7. Valid write data must be present and held stable during the latter portion of the R/$\overline{W}$ pulse. In a read cycle, the M48T86 outputs 8 bits of data during the latter portion of the DS pulse. The read cycle is terminated and the bus returns to a high impedance state upon a high transition on R/$\overline{W}$.

AS (Address Strobe Input). A positive going pulse on the Address Strobe (AS) input serves to demultiplex the bus. The falling edge of AS causes the address present on AD0-AD7 to be latched within the M48T86.

MOT (Mode Select). The MOT pin offers the flexibility to choose between two bus types. When connected to Vcc, Motorola bus timing is selected. When connected to V_{SS} or left disconnected, Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20K ohms.

DS (Data Strobe Input). The DS pin is also referred to as Read (RD). A falling edge transition on the Data Strobe (DS) input enables the output during a a read cycle. This is very similar to an Output Enable ($\overline{G}$) signal on other memory devices.

E (Chip Enable Input). The Chip Enable pin must be asserted low for a bus cycle in the M48T86 to be accessed. Bus cycles which take place without asserting $\overline{E}$ will latch the addresses present, but no data access will occur.

$\overline{IRQ}$ (Interrupt Request Output). The $\overline{IRQ}$ pin is an open drain output that can be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. $\overline{IRQ}$ returns to a high impedance state whenever Register C is read. The $\overline{RST}$ pin can also be used to clear pending interrupts. Because the $\overline{IRQ}$ bus is an open drain output, it requires an external pull-up resistor and connection to a power supply other than V_{CC}.

$\overline{RST}$ (Reset Input). The M48T86 is reset when the $\overline{RST}$ input is pulled low. With a valid V_{CC} applied and a low on $\overline{RST}$, the following events occur:

1. Periodic Interrupt Enable (PIE) bit is cleared to a zero. (Register B; Bit 6)
2. Alarm Interrupt Enable (AIE) bit is cleared to a zero. (Register B; bit 5)
3. Update Ended Interrupt Request (UF) bit is cleared to a zero. (Register C; Bit 4)
4. Interrupt Request (IRQF) bit is cleared to a zero. (Register C Bit 7)
5. Periodic Interrupt Flag (PF) bit is cleared to a zero. (Register C; Bit 6)
6. The device is not accessible until $\overline{RST}$ is returned high.
7. Alarm Interrupt Flag (AF) bit is cleared to a zero. (Register C; Bit 5)
8. The $\overline{IRQ}$ pin is in the high impedance state.
9. Square Wave Output Enable (SQWE) bit is cleared to zero. (Register B; Bit 3).
10. Update Ended Interrupt Enable (UIE) is cleared to a zero. (Register B; Bit 4)

$\overline{RCL}$ (RAM Clear). The $\overline{RCL}$ pin is used to clear all 114 storage bytes, excluding clock and control registers, of the array to FF(hex) value. The array will be cleared when the $\overline{RCL}$ pin is held low for at least 100ms with the oscillator running. Usage of this pin does not affect battery load.

R/$\overline{W}$ (Read/Write Input). The R/$\overline{W}$ pin is utilized to latch data into the M48T86 and provides functionality similar to $\overline{WR}$ in other memory systems.

ADDRESS MAP

The address map of the M48T86 is shown in Figure 8. It consists of 114 bytes of user RAM, 10 bytes of RAM that contain the RTC time, calendar and alarm data, and 4 bytes which are used for control and status. All bytes can be read or written to except for the following:

1. Registers C & D are read-only.
2. Bit 7 of Register A is read-only.
3. The high order bit of the seconds bytes is read-only.

The contents of the four register A, B, C, and D are described in the "Registers" section.

Table 3. Time, Calendar and Alarm Formats

Address	RTC Bytes	Range		
		Decimal	Binary	BCD
0	Seconds	0-59	00-3B	00-59
1	Seconds Alarm	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Minutes Alarm	0-59	00-3B	00-59
4	Hours, 12-hrs	1-12	01-0C AM 81-8C PM	01-12 AM 81-92 PM
	Hours, 24-hrs	0-23	00-17	00-23
5	Hours Alarm, 12-hrs	1-12	01-0C AM 81-8C PM	01-12 AM 81-92 PM
	Hours Alarm, 24-hrs	0-23	00-17	00-23
6	Day of Week (1=Sun)	1-7	01-07	01-07
7	Day of Month	1-31	01-1F	01-31
8	Month	1-12	01-0C	01-12
9	Year	0-99	00-63	00-99

TIME, CALENDAR, and ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar, and alarm registers are set or initialized by writing the appropriate RAM bytes. The contents of the ten time, calendar, and alarm bytes can be either Binary or Binary-Coded Decimal (BCD) format. Before writing the internal time, calendar,and alarm register, the SET bit (Register B; Bit 7) should be written to a logic "1". This will prevent updates from occurring while access is being attempted. In addition to writing the ten time, calendar, and alarm registers in a selected format (binary or BCD), the Data Mode (DM) bit (Register B; Bit 2), must be set to the appropriate logic level ("1" signifies binary data; "0" signifies Binary Coded Decimal (BCD data). All ten time, calendar, and alarm bytes must use the same data mode. The SET bit should be cleared after the Data Mode bit has been written to allow the Real Time Clock to update the time and calendar bytes. Once initialized, the Real Time Clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. Figure 9 shows the binary and BCD formats of the ten time, calendar, and alarm locations. The 24/12 bit (Register B; Bit 1) cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, a logic one in the high order bit of the hours byte represents PM. The time, calendar, and alarm bytes are always accessible because they are double buffered. Once per second theten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exists where seconds, minutes, hours, etc. may not correlate. However, the probability of reading incorrect time and calendar data is low. Methods of avoiding possile incorrect time and calendar reads are reviewed later in this text.

NON-VOLATILE RAM

The 128 general purpose non-volatile RAM bytes are not dedicated to any special function within the M48T86. They can be used by the processor program as non-volatile memory and are fully accessible during the update cycle.

Figure 4A. AC Testing Load Circuit

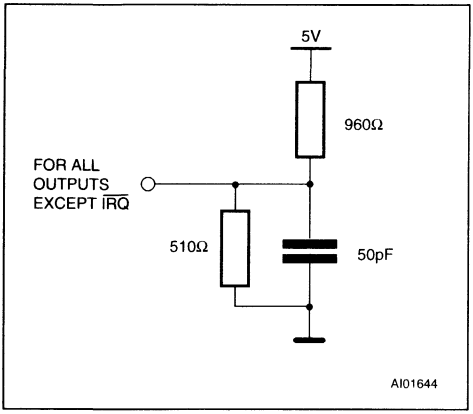
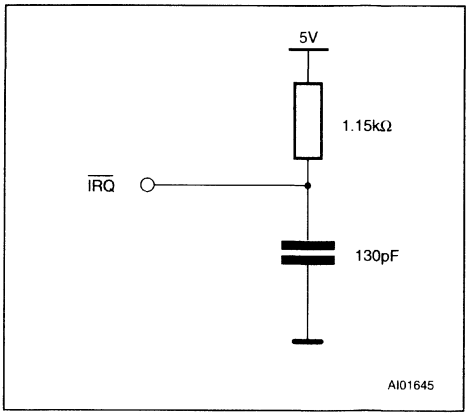


Figure 4B. AC Testing Load Circuit



AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Table 4. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		7	pF
C_{IO} (2)	Input / Output Capacitance	V_{OUT} = 0V		5	pF

Notes: 1. Effective capacitance calculated from the equation C = IΔt/ΔV with ΔV = 3V and power supply at 5V.
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} (1)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±1	µA
I_{CC}	Supply Current	Outputs open		15	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 4mA		0.4	V
	Output Low Voltage ($\overline{IRQ}$)	I_{OL} = 0.5mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Table 6. Power Down/Up Trip Points DC Characteristics (1) (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48T86)	4.0		4.35	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR} (2)	Expected Data Retention Time	10			YEARS

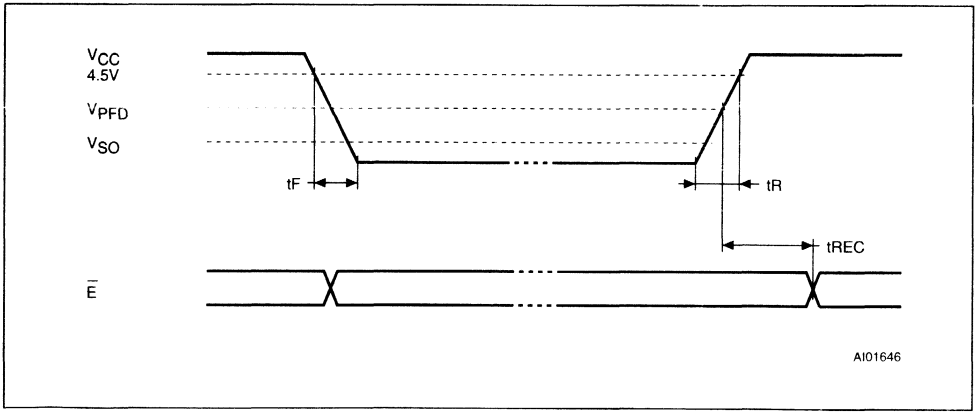
Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_F (1)	V_{CC} Fall Time	300		µs
t_R	V_{CC} Rise Time	100		µs
t_{REC}	V_{PFD} to $\overline{E}$ High	20	200	ms

Note: 1. V_{CC} fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD}.

Figure 5. Power Down/Up Mode AC Waveforms



INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt (alarm, periodic, update-in-progress) available to a processor. The alarm interrupt can be programmed to occur at rates from once per second to once per day. The periodic interrupt can be selected from rates of 500ms to 122µs. The update-ended interrupt can be used to indicate that an update cycle has completed.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a logic "1" to an interrupt-enable bit (Register B; Bit 6=PIE; Bit 5=AIE; Bit 4=UIE) permits an interrupt to be intialized when the event occurs. A zero in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level, although the

Table 8. AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	M48T86			Unit
		Min	Typ	Max	
t_{CYC}	Cycle Time	160			ns
t_{DSL}	Pulse Width, Data Strobe Low or R/$\overline{W}$ High	80			ns
t_{DSH}	Pulse Width, Data Strobe High or R/$\overline{W}$ Low	55			ns
t_{RWH}	R/$\overline{W}$ Hold Time	0			ns
t_{RWS}	R/$\overline{W}$ Setup Time	10			ns
t_{CS}	Chip Select Setup Time	5			ns
t_{CH}	Chip Select Hold Time	0			ns
t_{DHR}	Read Data Hold Time	0		25	ns
t_{DHW}	Write Data Hold Time	0			ns
t_{AS}	Address Setup Time	20			ns
t_{AH}	Address Hold Time	5			ns
t_{DAS}	Delay Time, Data Strobe to Address Strobe Rise	10			ns
t_{ASW}	Pulse Width Address Strobe High	30			ns
t_{ASD}	Delay Time, Address Strobe to Data Strobe Rise	35			ns
t_{OD}	Output Data Delay Time from Data Strobe Rise			50	ns
t_{DW}	Write Setup Time	30			ns
t_{BUC}	Delay Time before Update Cycle		244		ns
t_{PI} (1)	Periodic Interrupt Time interval	–	–	–	
t_{UC}	Time of Update Cycle		1		µs

Note: 1. See Table 9.

INTERRUPTS (cont'd)

interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the related flag bit (Register C; Bit 6=PF; Bit 5=AF; Bit 4=UF) is set to a logic "1". These flag bits are set independent of the state of the corresponding enable bit in Register B and can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bits are status bits which software can interrogate as necessary.

When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as all are cleared each time Register C is read. Double latching is included with Register C so that bits which are set, remain stable throughout the read cycle. All bits which are set high are cleared when read. Any new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two, or three bits can be set when reading Register C. Each utilized flag bit should be examined when read to ensure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The $\overline{IRQF}$ bit (Register C; Bit 7) is a "1" whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic "1" in the IRQF bit indicates that one or more interrupts have been initiated by the M48T86. The act of reading Register C clears all active flag bits and the IRQF bit.

Figure 6. Intel Bus Read Mode AC Waveforms

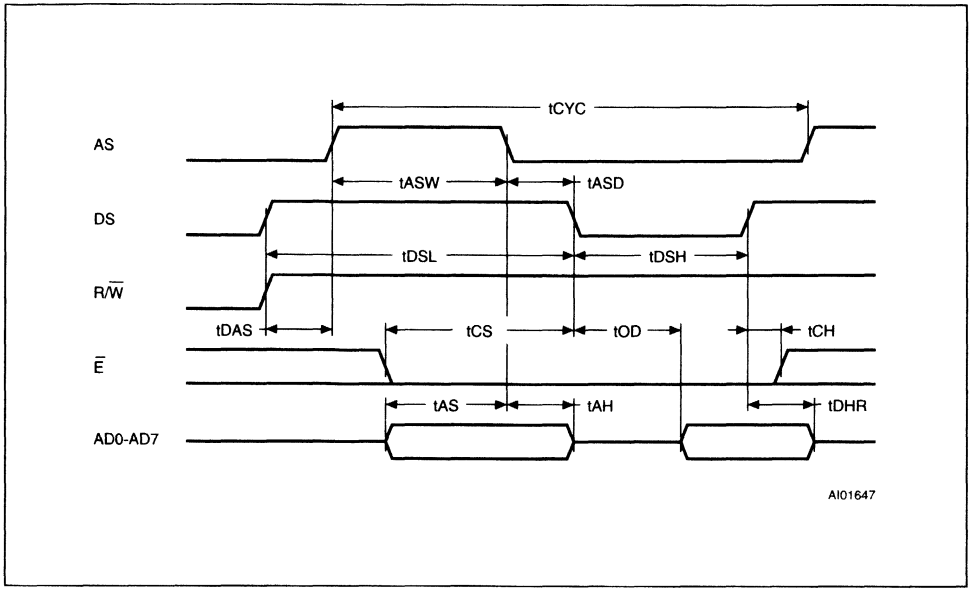


Figure 7. Intel Bus Write Enable AC Waveforms

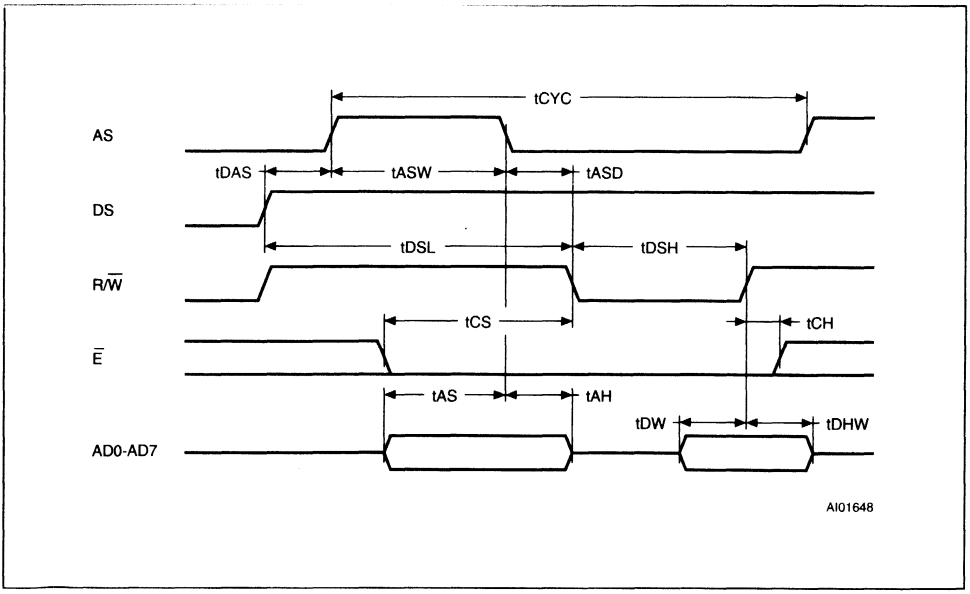
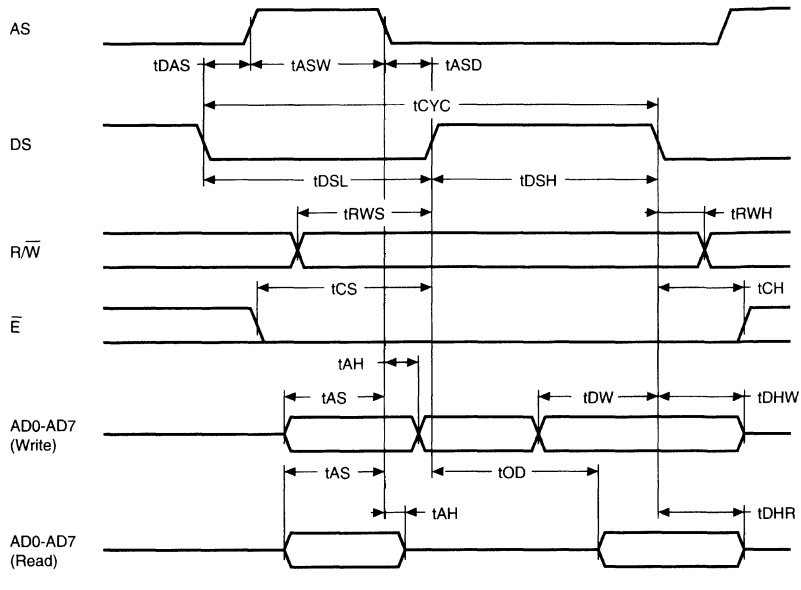


Figure 8. Motorola Bus Read/Write Mode AC Waveforms



PERIODIC INTERRUPT

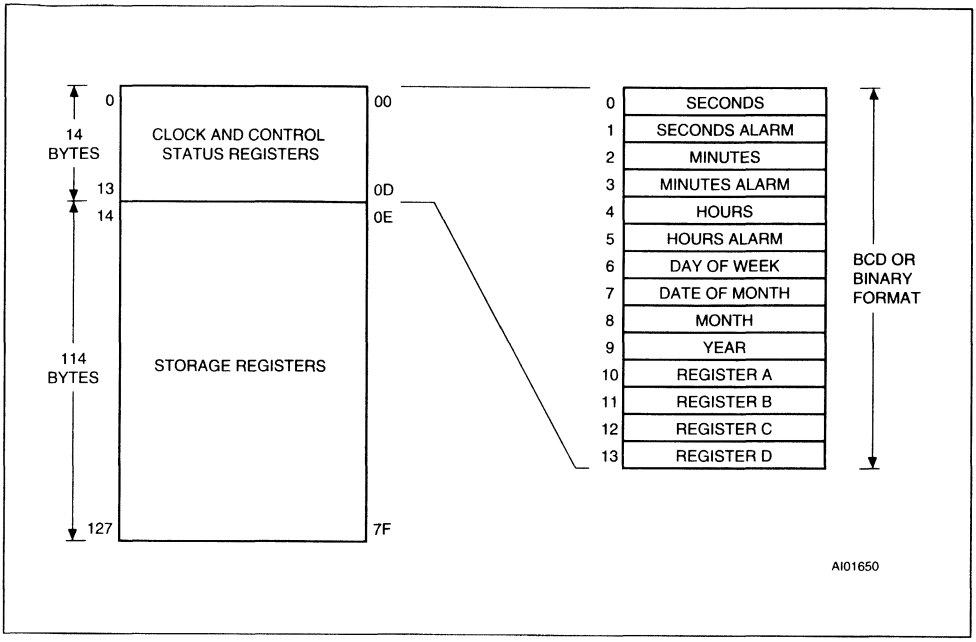
The periodic interrupt will cause the IRQ pin to go to an active state from once every 500 ms to once every 122µs. This function is separate from the alarm interrupt which can be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 8). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The periodic interrupt is enabled by the PIE bit (Register B; Bit 6). The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

ALARM INTERRUPT

The alarm interrupts provides the system processor with an interrupt when a match is made between the RTC's hours, minutes, and seconds bytes and the corresponding alarm bytes. The alarm interrupt is also active in the battery back-up mode providing a system "wake-up" capability.

Thee three alarm bytes can be used in two ways. First when the alarm time is written in the appropriate hours, minutes, and seconds alarm locations the alarm interrupt is initiated at the specified time each day if the Alarm Interrupt Enable bit (Register B; Bit 5) is high. The second use is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at logic "1". An alarm will be generated each hour when the "don't care" is are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hour and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Figure 9. Address Map



UPDATE CYCLE INTERRUPT

After each update cycle, the update cycle ended flag bit (UF) (Register C; Bit 4) is set to a "1". If the update interrupt enable bit (UIE) (Register B; Bit 4) is set to a "1", and the SET bit (Register B; Bit 7) is a "0", then an interrupt request is generated at the end of each update cycle.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 3. The purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS3-RS0 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 9. The SQW frequency selection shares it's 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin can be turned on and off under program control with the square wave enabled (SQWE).

OSCILLATOR CONTROL BITS

When the M48T86 is shipped from the factory the internal oscillator is turned off. This feature prevents the lithium energy cell from being discharged until it is installed in a system. A pattern of "010" in Bits 4-6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of "11X" will turn the oscillator on, but holds the countdown-chain of the oscillator in reset. All other combinations of Bits 4-6 keep the oscillator off.

Table 9. Square Wave Frequency/Periodic Interrupt Rate

Register A Bits				Square Wave		Periodic Interrupt	
RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	0	0	0	None		None	
0	0	0	1	256	Hz	3.90625	ms
0	0	1	0	128	Hz	7.8125	ms
0	0	1	1	8.192	kHz	122.070	us
0	1	0	0	4.096	kHz	244.141	us
0	1	0	1	2.048	kHz	488.281	us
0	1	1	0	1.024	kHz	976.5625	us
0	1	1	1	512	Hz	1.953125	ms
1	0	0	0	256	Hz	3.90625	ms
1	0	0	1	128	Hz	7.8125	ms
1	0	1	0	64	Hz	15.625	ms
1	0	1	1	32	Hz	31.25	ms
1	1	0	0	16	Hz	62.5	ms
1	1	0	1	8	Hz	125	ms
1	1	1	0	4	Hz	250	ms
1	1	1	1	2	Hz	500	ms

UPDATE CYCLE

The M48T86 executes an update cycle once per second regardless of the SET bit (Register B; Bit 7). When the SET bit is asserted, the user copy of the double buffered time, calendar,a and alarm bytes is frozen and will not update as the time increments. However, the time countdown-chain continues to update the internal copy of thee buffer. This feature allows accurate time to be maintained, independent of reading and writing the time, calendar, and alarm buffers. This also guarantees that the time and calendar information will be consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code is present in all three positions.

There are three methods of accessing the real time clock that will avoid any possibility of obtaining inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999ms are available to read valid time and date information. if this interrupt is used, the IRQF bit (Register C; Bit 7) should be cleared before leaving the interrupt routine.

A second method uses the Update-In-Progress (UIP) bit (Register A; Bit 7) to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 us later. If a low is read on the UIP bit, the user has at least 244 us before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit is set high between the setting of the PF bit (Register C; Bit 6). Periodic interrupts that occur at a rate greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be completed within $1/(t_{PL/2} + t_{BUC})$ to ensure that data is not read during the update cycle.

Figure 10. Update Period Timing and UIP

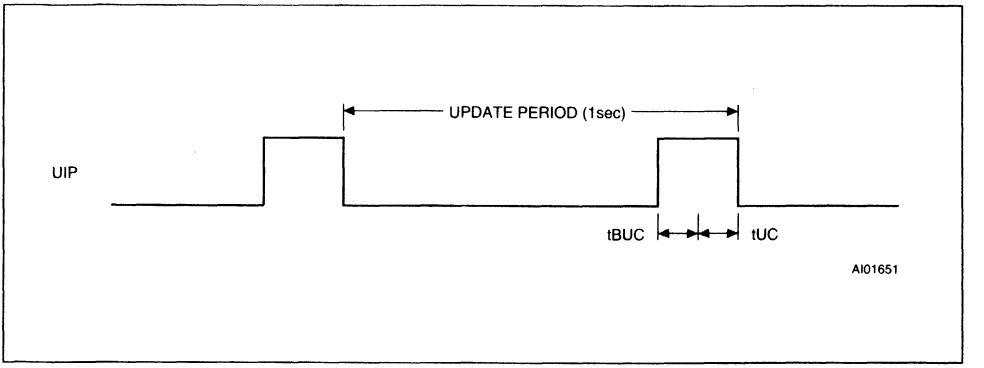
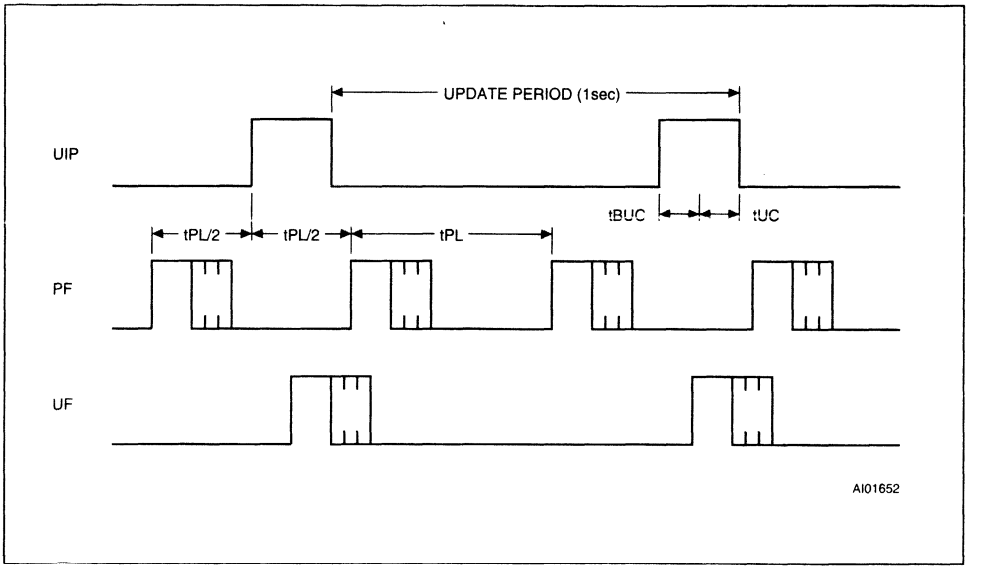


Figure 11. Update-ended/Periodic Interrupt Relationship



REGISTER A

MSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	OSC2	OSC1	OSC0	RS3	RS2	RS1	RS0

UIP. Update in Progress

The Update in Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is one the update transfer will not occur for at least 244 us. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by RST. Writing the SET bit in Register B to a " 1" inhibits any update transfer and clears the UIP status bit.

OSC0, OSC1, OSC2. Oscillator Control

These three bits are used to control the oscillator and reset the coutdown chain. A pattern of 010 enables operation by turning on the oscillator and enabling the divider chain. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When 010 is written, the RTC begins it's first update after 500ms.

RS3, RS2, RS1, RS0

These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user may do one of the following:

1. Enable the interrupt with the PIE bit;

or

2. Enable the SQW output with the SQWE bit;

or

3. Enable both at the same time and same rate;

or

4. Enable neither.

Table 9 lists the periodic interrupt rates and the square wave frequenciies that may be chosen with the RS bits. These four read/write bits are not affected by RST.

REGISTER B

MSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET

When the SET bit is a zero, the update transfer functions normally by advancing the coutns once per second. When the SET bit is written to a one, any update transfer is inhibited and the program may initialize the time and calendar bytes without an update occurring. Read cycles can be executed in a similar manner. SET is a read/write bit which is no modified by RST or internal functions of the M48T86.

PIE. Periodic Interrupt Enable

The Periodic Interrupt Enable bit (PIE) is a read/write bit which allows the Periodic Interrupt Flag (PF) bit Regiser C to cause the IRQ pin to be driven low. When the PIE bit is ser to one, periodic interrupts are generated by driving the IRQ pin low at a rate specified by the RS3-RS0 bits of Register A. A zero in the PIE bit blocks the IRQ output output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is no modfied by any internal M48T86 functions, but is cleared to zero on RST.

AIE. Alarm Interrupt Enable

The Alarm Interrupt Enable (AIE) bit is a Read/Write bit which, when set to a one, permits the Alarm Flag (AF) bit in Register C to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a "don't care" alarm code of binary 1XXXXXXX. When the AIE bit is set to zero, the AF bit does not initate the IRQ signal. The RST pin clears AIE to zero. The internal functions of the M48T86 do not affect the AIE bit.

UIE. Update Ended Interrupt Enable

The Update Ended Interrupt Enable (UIE) bit is a read/write bit which enables the Update End Flag (UF) bit in Register C to assert IRQ. A transition low on the RST pin or the SET bit going high clears the UIE bit.

SQWE. Square Wave Enable

When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal is driven out on the SQW pin. The frequency is determined by the rate-selection bits RS3-RS0. When the SQWE bi is set to zero, the SQW pin is held low. The SQWE bit is cleared by the RST pin. SQWE is a read/write bit.

DM. Data Mode

The Data Mode (DM) bit indicates whether time and calendar information are in binary or BCD format. The DM bit is set by the program to the appropriate format and can beread as required. This bit is not modified by internal function or RST. A one in DM signifies binary data and a zero specifies Binary Coded Decimal (BCD) data.

24/12

The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is read/write and is not affected by internal functions or RST.

DSE. Daylight Savings Enable

The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when set to a one. On the first Sunday in April the time increments from 1:59:59AM to 3:00:00 AM. On the last Sunday in October, when the time reaches 1:59:59 AM, it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or RST.

REGISTER C

MSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF. Interrupt Request Flag

The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF=PIE=1

AF=AIE=1

UF=UIE=1

(i.e. IRQF=PF*PIE+AF*AIE+UF*UIE)

PF. Periodic Interrupt Flag

The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3-RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. The IRQ isgnal is active and will set the IRQF bit. The PF bit is cleared by a RST or a software read of Register C.

AF. Alarm Flag

A one in the AF (Alarm Interrupt Flag) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the IRQ pin will go low and a one will appear in the IRQF bit. A RST or a read of REgister C will clear AF.

UF. Update Ended Interrupt Flag

The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to a one, the one in the UF bit causes the IRQF bit to be a one. This will assert the IRQ pin. UF is cleared by reading Register C or an RST.

BIT 0 through 3. Unused Bits

Bit 3-Bit 0 are unused. These bits always read zero and cannot be written.

REGISTER D

MSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

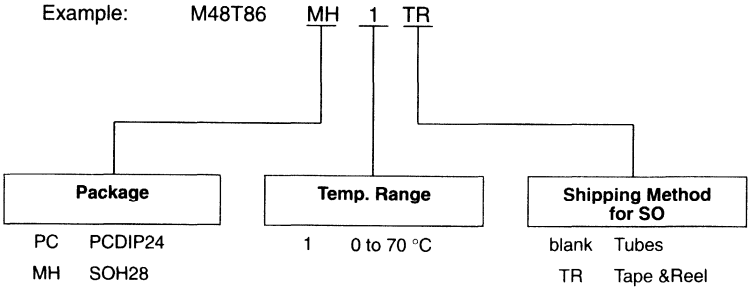
VRT. Valid Ram And Time

The Valid RAM and Time (VRT) bit is set to the one state by SGS-THOMSON prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium cell is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by RST.

BIT 0 through 6. Unused Bits

The remaining bits of Register D are not usable. They cannot be written and when read, they will always rea zero.

ORDERING INFORMATION SCHEME



The SO and battery packages are shipped separately in plastic anti-static tubes. The SO package is also available to ship in Tape & Reel form. For the 28 lead SO, the battery package part number is "M4T28-BR12SH1".

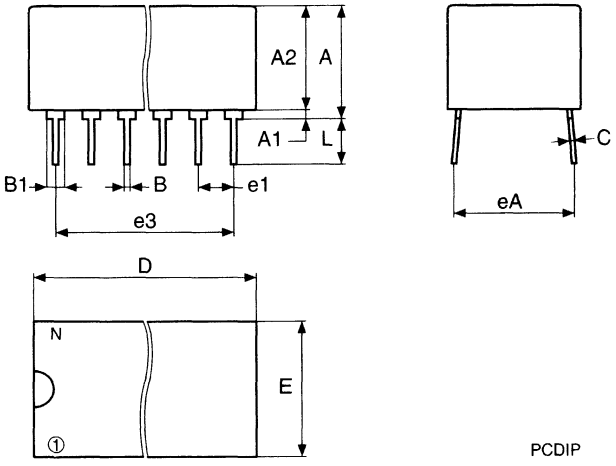
For a list of available options refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP24 - 24 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.36	8.89		0.329	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		34.29	34.80		1.350	1.370
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		25.15	30.73		0.990	1.210
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	24			24		

PCDIP24



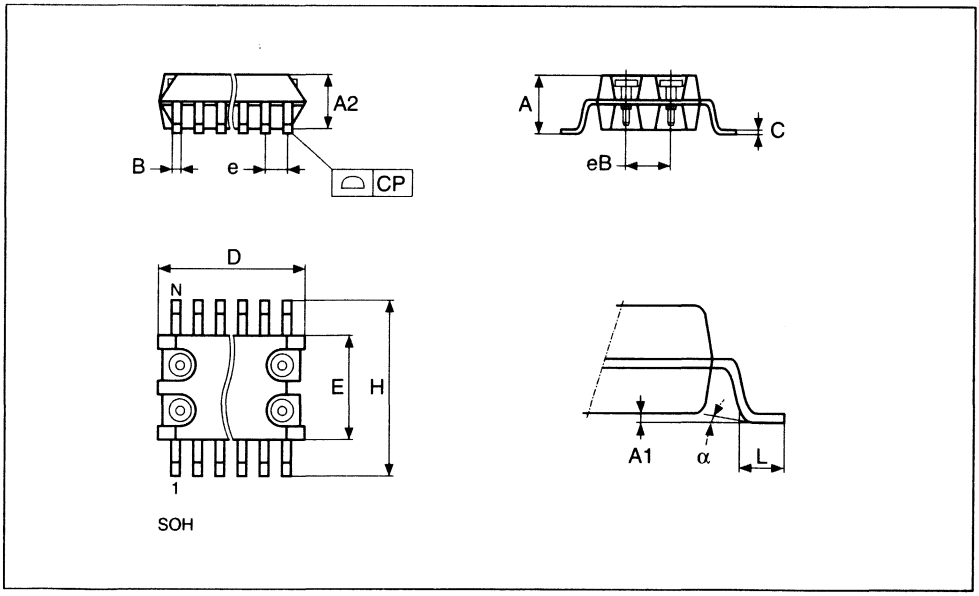
PCDIP

Drawing is not to scale

SOH28 - 28 lead Plastic Small Outline, battery SNAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

SOH28

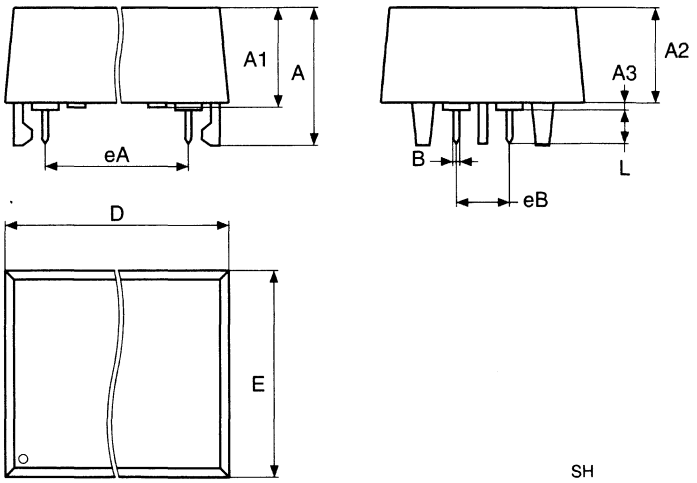


Drawing is not to scale

SH28 - SNAPHAT Housing for 28 lead Plastic Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

SH28



SH

Drawing is not to scale

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